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Issue 26/2005

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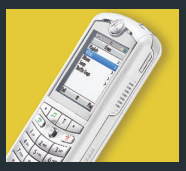

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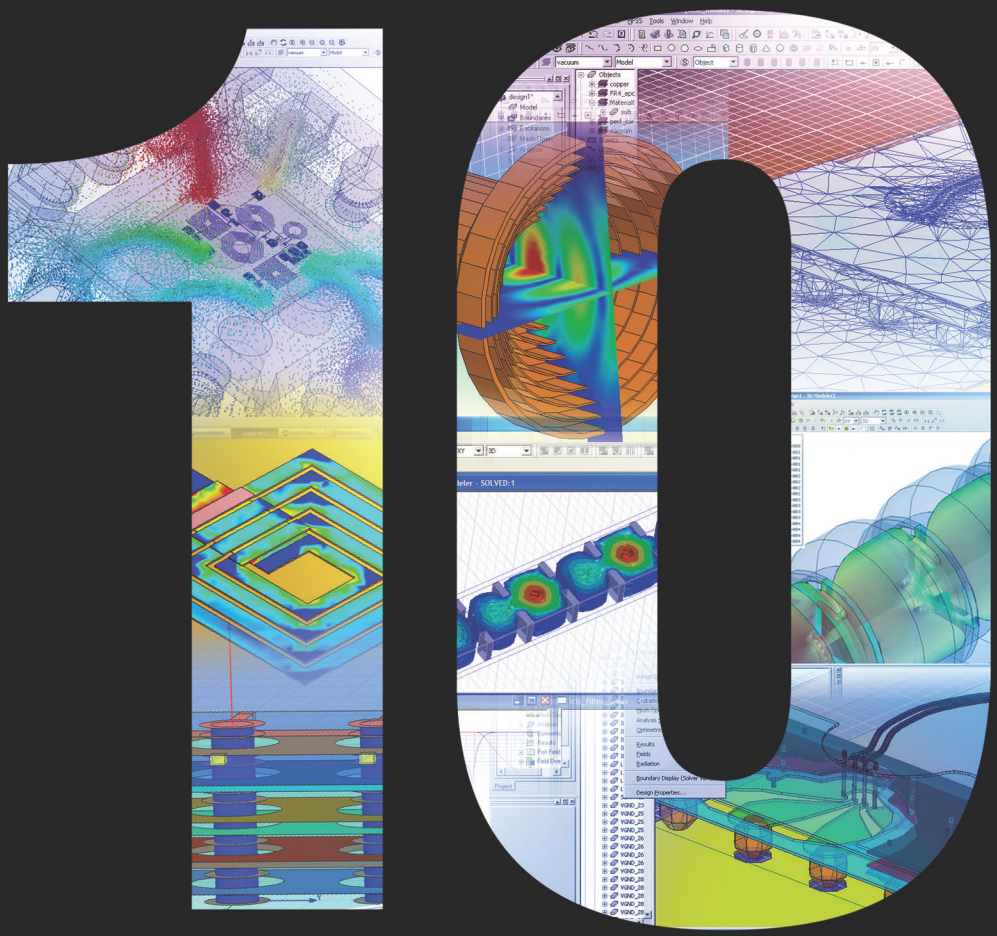

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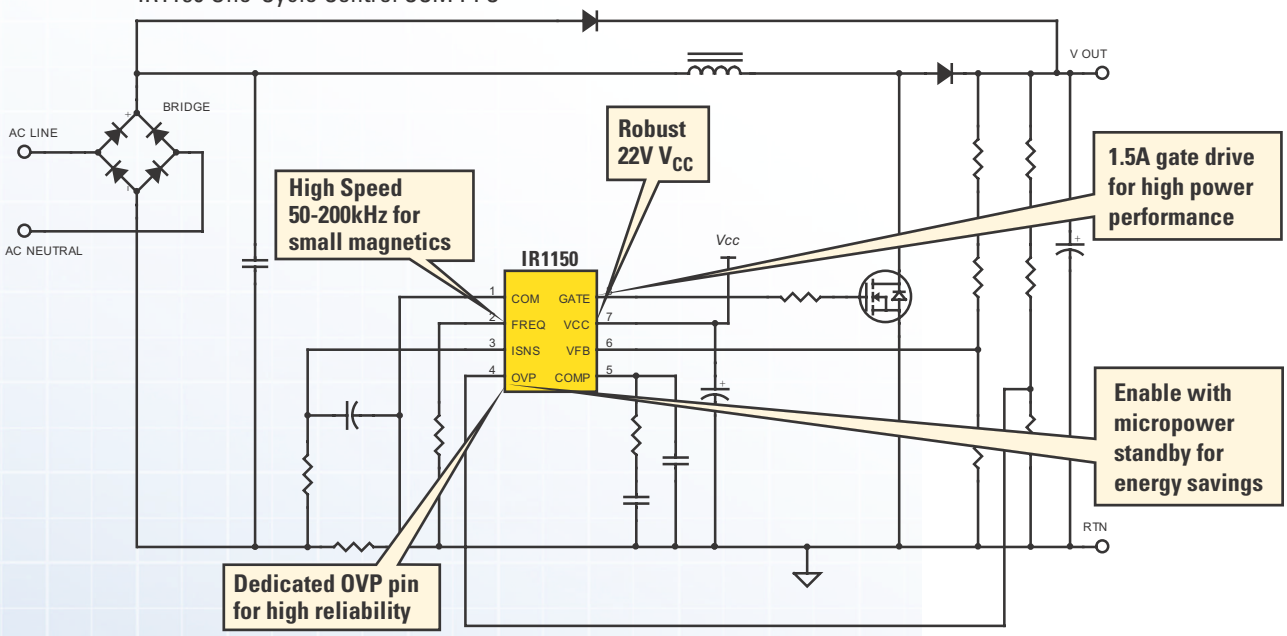

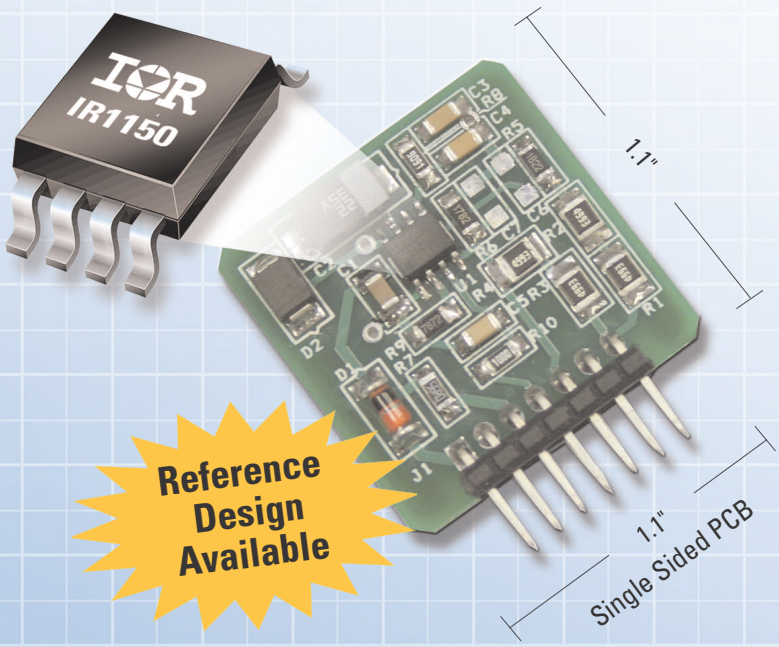

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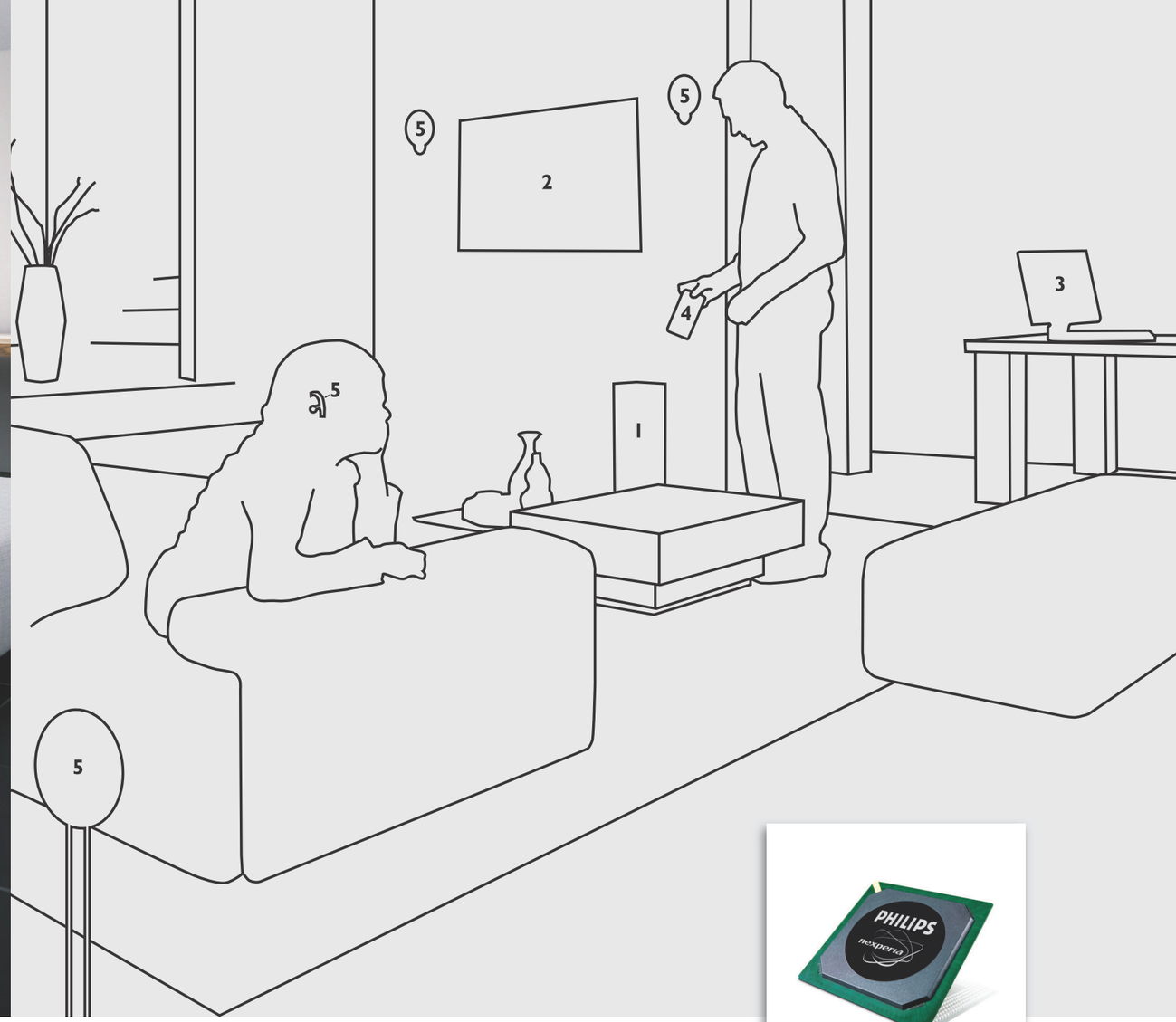

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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A New Approach to Streamlining the Application of Advanced Technologies

Today's increasing silicon complexity drives engineers to continually leverage the latest advances in electronic design. However, no company can afford to have its design teams consuming time and effort adopting individual technologies. Instead, organizations need to focus precious engineering resources where they add the most value—differentiating the company's designs. Additionally, in today's fast-paced markets, missed schedules can mean lost market opportunities. Cadence recognizes that to start designing right away, designers need a proven infrastructure—proven on the types of designs they'll be doing and incorporating the kind of IP they'll be incorporating—with typical application hurdles already flattened. This is the essence of the Cadence Kits approach.

A Cadence Kit is a documented methodology built on a set of platform flows applied to a reference design, which is enabled by standards-based IP and packaged with applicability training. Each kit starts with a reference design—a real design representing a specific vertical market.

The reference design incorporates IP that is integrated and validated with the platform flows. One of the biggest challenges has been the difficulty of using IP in the design process. By building on platform flows and a reference design, Cadence Kits greatly simplify the integration, reuse and enablement of IP.

DELIVERING ON THE KITS APPROACH

The first Cadence Kit focuses on analog/mixed-signal (AMS) because of its pervasiveness across markets, including wireless, wired networking, and personal entertainment electronics. The AMS Methodology Kit minimizes risk by targeting key challenges identified by customers in these markets:

- Fragmented design processes that prevent teams from effectively verifying designs across the analog and digital design domains
- Large quantities of data and long simulations, which hamper modeling, extraction and re-simulation of parasitics
- The challenge of managing multiple power supplies through all stages of design as well as reusing and migrating AMS blocks—both of which demand a predictable methodology

The Cadence AMS Methodology Kit addresses these design challenges by delivering a verified methodology, enabling IP, and applicability training—all demonstrated on an end-to-end mixed-signal design.

The AMS Methodology Kit executes a "meet in the middle" design approach that achieves an optimum balance between the needs for speed and for silicon accuracy. It also establishes a design process that allows teams to work with the analog/mixed-signal content in the context of the complete design—from concept to silicon.

The kit gives designers control of parasitic effects from first-cut route and top-level parasitic extraction evolving to block-level and targeted post-layout re-simulation. It addresses reuse and migration of analog/mixed-signal blocks through a repeatable block creation method. In addition, the AMS Methodology Kit helps teams tackle low-power designs by managing multiple power supplies through a top-down methodology for defining voltage supplies.

For more information on how Cadence Kits enable you to simplify the application of EDA technology for greater design productivity, visit www.cadence.com/kit_info.

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Cadence tailors tools for "elite" digital designers

The company's GXL series of IC tools targets the so-called "elite" ASIC/SOC designers—those working on high-speed designs at 65 nm and below.
→ www.edn.com/article/CA6288819

NOC, NOC, NOCing on heaven's door: Beyond MPSOCs

A report from the seventh-annual International Symposium on System-on-Chip design.
→ www.edn.com/article/CA6289284

ADC blazes at 190M samples/sec, but sips power

Targeting applications in wireless communications, video and imaging, test and measurement, and instrumentation, the ADS5546 from Texas Instruments offers 73.2-dBFS SNR and 84-dBc SFDR (spurious-free dynamic range) at the maximum sample rate of 190M samples/sec.
→ www.edn.com/article/CA6287412

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FROM THE VAULT

Articles and extras from the EDN *archives that relate to this issue's contents.*

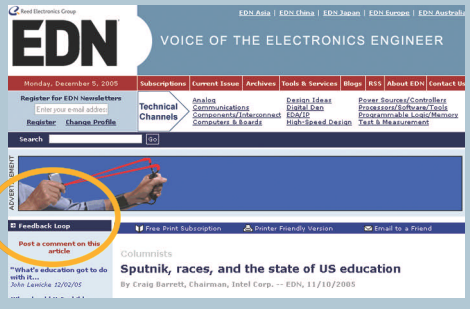
The hot 100 products of 2005 (pg 35):

The hot 100 products of 2004
→ www.edn.com/article/CA486570

The hot 100 products of 2003
→ www.edn.com/article/CA339713

Prying Eyes: Thinking different (pg 32):

Mac (under) the knife: Piecing together the PowerPC puzzle.
→ www.edn.com/article/CA6255047



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→ www.edn.com/article/CA6280032

And some people think we shouldn't have published this recent Design Idea:
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BY MAURY WRIGHT, EDITOR IN CHIEF

High-stakes partnering: Who has the hole card?

It seems there have been a number of tech partnerships of late in which it's tough to figure out which partner is playing from a position of strength and which might be bluffing. Like poker players, tech companies play all-in for their own benefit. But partnerships often obscure the win-at-all-costs mentality. Take the Qualcomm partnership with Samsung announced in late November. Samsung, the handset maker, has been one of Qualcomm's biggest customers. Now, Samsung will be a fab partner, building cell-phone chips for Qualcomm. Is this a case of Qualcomm simply finding the best manufacturing partner out there? I'm not so sure.

Surely some amount of the success that Samsung has enjoyed in the handset business comes from the company's decision to endorse Qualcomm's CDMA technology. But CDMA-handset makers have paid a premium relative to their GSM (Global System for Mobile communications) counterparts because of the vast CDMA intellectual property that Qualcomm owns. Likewise, CDMA carriers have paid the Qualcomm tax as well, albeit they've arguably enjoyed more efficient networks.

Some in the CDMA camp—notably Samsung and carriers in Korea—seem determined not to be beholden to Qualcomm—or anyone else—for next-generation standards. As I covered in a recent feature story, Korea has actively sought to develop the country's own 4G mobile standard, WiBro, and WiBro may or may not align precisely with a WiMax standard (**Reference 1**). The Korean contingent was especially miffed when Qualcomm cut China a lower cost deal to win current-generation mobile business in what industry insiders commonly consider the biggest opportunity in the global market.

So, Qualcomm faced a partner that could've quickly turned into a competitor. Samsung has refined its IC-manufacturing capabilities using flash memory as a driver, and the company has become world-class in every way. Samsung could clearly be a threat in next-generation handset chips.

Now, however, Samsung will be making chips for Qualcomm. The companies haven't specified the scale of the deal. Qualcomm has long been among the biggest fabless companies, relying primarily on TSMC as a foundry. You could argue that Qualcomm simply needs an alternative source and additional capacity. In fact, that scenario is likely true. Presumably, Qualcomm will have additional opportunities as GSM carriers roll out wideband-CDMA networks and as some portion of Qualcomm's IP portfolio enters the larger GSM segment.

There are also many reasons to believe that Samsung is an excellent choice as a fab partner. The company has a solid technology base today. And Samsung is allied with IBM, Chartered, and Infineon to develop 65-nm- and finer-grain processes. Essentially, a relationship with Samsung could blossom into a manufacturing relationship with all four partners.

Still, I keep coming back to Samsung as a threat to Qualcomm and as a company unhappy with its share of CDMA cellular profits. By making a deal with Samsung, Qualcomm can keep the emerging giant solidly in the CDMA camp. Samsung will get a chance at a share of the profits as all flavors of CDMA proliferate. Qualcomm might even win over Samsung for support for Qualcomm's MediaFlo technology for video multicast to handsets despite the fact that Korea is already deploying competing technologies.

Then again, I don't think Samsung is all-in with this one deal. In fact, the company just demonstrated a WiBro-based phone and PDA at the 2005 APEC IT Exhibition (www.apecitkorea.org/eng/index.asp). EDN

REFERENCE

1 Wright, Maury, "WiMax wireless broadband: Fixed-flavor questions abound, mobile lurks," *EDN*, March 31, 2005, pg 44, www.edn.com/article/CA512128.

Editor's note

I hope you enjoy Bill Schweber's article on quantum cryptography on pg 41. Bill has always produced excellent articles, and this one is no exception. And it's on a fascinating subject. Bill, however, has decided to leave *EDN* for a new challenge. We will miss him (and I'm sure you will, too), and we thank him for all of his years of great work.

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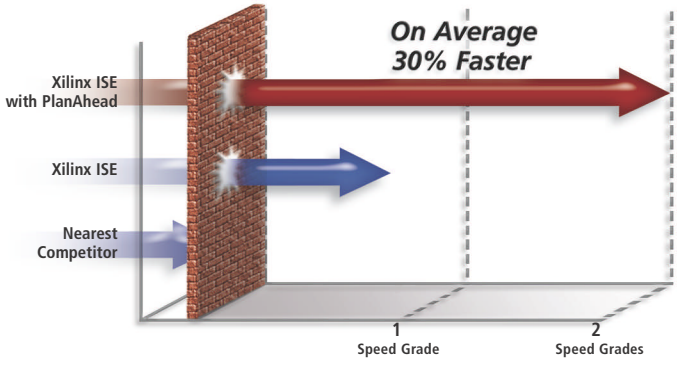

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* CMP: June 2005 FPGA EDA Survey

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Q. *My clock is accurate to 1 ppm—what could possibly need improvement?*

A. The phase noise or jitter. The performance of any ac sampling system is critically dependent on the use of a sampling clock with adequately low jitter.

A quarter of a century ago I was technical advisor to a Parliamentary Committee on CB Radio. We met at Westminster Hall in the Houses of Parliament in London, almost directly under Big Ben, whose chimes punctuated our deliberations. I frequently used Big Ben as an example when explaining the importance of various features of clocks and oscillators.

In a sampled data system, a changing signal is sampled at regular intervals and the signal is processed by performing calculations on the samples. If an oscillator has jitter, the clock edges occur earlier or later than they would in a jitter-free clock. The frequency accuracy is unaffected, only the exact timing of individual transitions varies.

If an edge comes early, the signal being sampled will not yet have reached its correct value, and if it comes late, the signal will have moved on—so to achieve accuracy in a sampled system it is important to have adequately low jitter on the system clock. In fact, frequency accuracy is often far less important. Obviously, the faster the sampled signal is changing, the greater the error will be for a given amount of jitter. The clock frequency is irrelevant—it is the frequency of the analog signal being sampled (in the case of the ADC) or signal being synthesized (in the case of the DAC) that matters.

Although the problem can be significant at quite modest signal frequencies (I have memories of digital audio systems with performance devastated by inappropriate clock oscillators—one a 555 timer, another an interrupt-driven microprocessor) it becomes critical in modern digital radios using IF sampling at signal frequencies of tens or hundreds of MHz. To give numbers, a perfect ADC (no imperfections of any sort) working with a 100 MHz signal and a clock with one picosecond (1E-12 seconds) rms jitter cannot achieve a resolution greater than 10 bits.

Links to information on the relevant formula, low noise clock circuits, and circuit techniques that ensure a low clock jitter signal is not degraded before it reaches the circuits it drives, are on the website below. A simple illustration of the difference between clock accuracy and clock jitter is to consider what would happen if Big Ben's hands always pointed to the exact time, but the chime occurred randomly up to five minutes early or late.

To learn more on accurately timing clocks, Go to: http://rbi.ims.ca/4402-501

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

raq@reedbusiness.com

The space-age material for the limited space age.

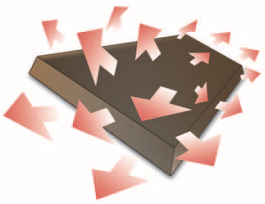
— *or* —

Why natural graphite is the best thermal solution for designing compact electronic devices.

As electronics get smaller and faster, design space becomes more critical. There simply is not room for traditional electronic cooling devices. Heat sinks, heat pipes and fans add weight, take up space, and are noisy. Traditional heat spreaders made of Cu and Al do not possess the properties for moving heat in a controlled, directional fashion that causes a shielding effect. And in compact devices you can not afford to have heat move from one source and adversely affect another. The solution? Expanded natural graphite – namely eGraf® SpreaderShield™ Heat Spreaders and eGraf® Fredda™ 3-Dimensional Heat Spreaders.

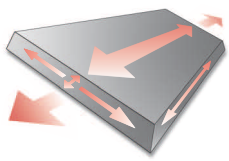
eGraf® materials are the latest technology available from GrafTech – global experts in expanded natural graphite thermal solutions. Expanded natural graphite solves problems associated with traditional heat management options. Compared to typical Al alloys, eGraf® components exhibit up to 200% higher thermal conductivity. The most dynamic characteristic of natural graphite is that it is anisotropic. Heat moves through it 2-dimensionally in an orderly fashion. The in-plane thermal conductivity is tailorable up to 500 W/mK and the through-plane in the range of 5-10 W/mK. This allows engineers the ability to direct heat in the x-y plane. The result, our material spreads heat and also creates a thermal shielding barrier to keep heat from affecting other components. Some traditional Cu or Al spreaders cannot do this.

Heat Transfer Dramatization

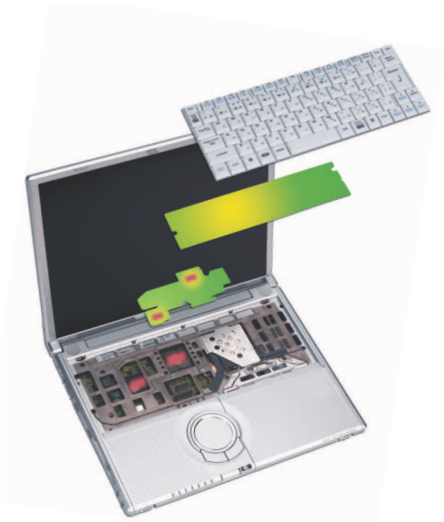


Isotropic Cu or Al has no thermal direction control or thermal shielding capability.

VS



Anisotropic eGraf® SpreaderShield™ material has full thermal direction control and thermal shielding capability.



eGraf® materials eliminated the need for fan, heat pipes and heat sinks.

eGraf® offers an array of solutions for engineers faced with space, weight and thermal reliability issues. eGraf® SpreaderShield™ material is a thin sheet of flexible graphite that fits where traditional heat spreaders can not. It can be tailorable up to 500 W/mK and can be die-cut to fit applications of any size or shape. eGraf® expanded natural graphite's pliable qualities allow it to conform to any design. It is available in a variety of thicknesses and useable at temperatures up to 400°C and lower than -40°C.

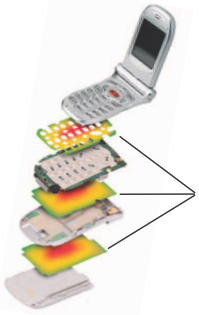
For more complex 3-dimensional shapes, we laminate our eGraf® SpreaderShield™ material with a thin sheet of Al foil to hold form, creating eGraf® Fredda™, a 3-Dimensional Heat Spreader. eGraf® Fredda™ materials can conduct, spread and sink heat to the outer case of an electronic device for sealed environments. This can eliminate the need for heat pipes, heat sinks and fans in low and ultra low voltage applications, resulting in decreased assembly weight of those components up to 50%.

eGraf® Fredda™ material

eGraf® SpreaderShield™ material

Customized to fit your needs
200% better thermal performance than Al and
80% lighter than Cu

What are you designing? eGraf® SpreaderShield™ and eGraf® Fredda™ materials are already being used in ultra low/low voltage notebook computers, ruggedized computers, PDPs, LCDs, LEDs, audio amplifiers, avionics, consumer electronics, PDAs, smart cell phones, medical devices and much more.



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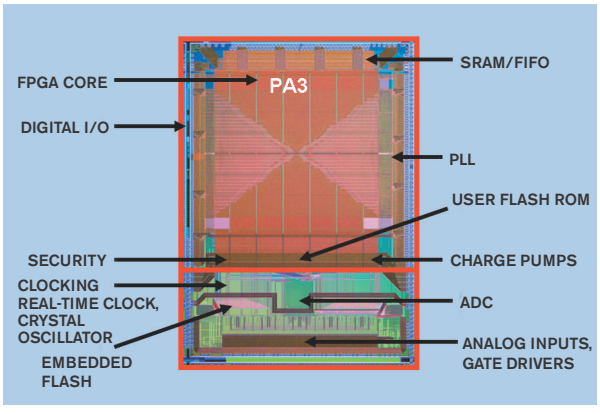
LIGHTER

Device incorporates mixed-signal circuitry

Actel Corp has announced the Fusion PSC (programmable system chip), which incorporates mixed-signal analog, flash memory, and FPGA fabric on a single die. The company has also released design software that it claims makes a significant stride toward the FPGA industry's dream of allowing software designers to program FPGAs.

"The big FPGA companies out there today are creating larger and larger FPGAs, primarily with digital logic on board, memory, and some processor capability, but they severely lack the ability to put analog and nonvolatile memory onto those advanced nodes," says Martin Mason, director of silicon-product marketing at Actel. "Our customer base is telling us they'd like to see more integration and more functions, not just more gates, for less than $20. They'd like to start interfacing into the real world—into analog."

The first device in the family, the AFS600, combines a configurable 12-bit SAR (successive-approximation-register) ADC handling frequencies as high as 600k samples/sec, with 600,000 system gates' worth of FPGA fabric and 512 kbytes of embedded flash. The analog block supports MOSFET-gate-driver output and multiple analog inputs from



The Fusion PSC devices mix an analog block with embedded flash and an FPGA fabric.

−12 to +12V with an optional prescaler.

Like other Actel devices, the Fusion devices are nonvolatile and flash-based, which typically offers a greater degree of content security and low power than SRAM-based devices. Mason says that, with the analog block, along with nonvolatile memory and programmable fabric, new devices suit use in power- and temperature-management, motor- and motion-control, system-initialization and -configuration, and storage applications, and they can serve as power-gatekeeper devices for low power and clocking.

Actel added the analog block to the bottom of the Fusion die and shielded it from the digital content to ensure that it is less susceptible to interference. Actel plans to eventually offer a radiation-tolerant version of the device to make it more attractive for automotive and even military and aerospace applications. The company offers a library of digital cores, including the ARM7 TDMI-S microprocessor, to help customers configure Fusion for those applications. Actel has also added a new "pick-and-click" Microsoft Wizard-like interface to its Libero FPGA-design software kit.

With Libero's CoreConsole, designers can program Fusion devices by clicking through three windows in the wizard. With a window, users add IP (intellectual-property) blocks to the device. They then move to a second window to floorplan and stitch the blocks together. The third click generates RTL for the design and a testbench for simulation.

Actel also offers a Fusion starter kit for $349. The kit includes an evaluation board with a set of MOSFETs for driving and controlling external voltages. It also includes multicolor LEDs for demonstrating PWM effects. Actel's AFS600 Fusion PSCs are available now. Actel plans to follow up with devices that have 90,000, 250,000, and 1.5 million system gates. Prices for the devices start at less than $5 (250,000 minimum).

—by Michael Santarini

▷**Actel Corp**, www.actel.com.

FEEDBACK LOOP

"In the global economy, smart American kids can do a lot better than innovating for companies and a government that value them less than plumbers."

John Lewicke, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6280033. Add your comments.

FPGA-physical-synthesis tool knows the fastest routes

Synplicity boasts that, in a single pass, its new graph-based FPGA-physical-synthesis tool uses inside knowledge of FPGA architectures to deliver a 5 to 20% performance improvement over the company's popular logic-synthesis tool. In addition, the company claims, 90% of all routed nets fall within 10% of final timing correlation. The new tool, Synplify Premier, will replace the company's Amplify physical-synthesis tool and become Synplify's top-of-the-line FPGA-synthesis tool.

The key to the tool's performance boost is its graph-based physical-synthesis engine, says Jeff Garrison, the company's director of FPGA-product marketing. Because FPGAs are prerouted, they limit the paths you can take between two functions. Synplicity has turned that architectural shortcoming into a design advantage by doing detailed analyses of the interconnect within certain FPGA families, Garrison says. Synplify Premier's graph-based engine has access to that information, which it uses to accurately find the fastest route to interconnect blocks within the FPGA.

Most FPGA-physical-synthesis routers use proximity-based techniques originally designed for ASICs. Proximity-based routers attempt to place functions next to or close to each other to reduce the length of the interconnect. "But in an FPGA, placing one function right next to another function may not be the fastest route between the two functions," Garrison says. "It's like commuting to work: You sometimes drive a bit out of the way to get to work faster."

In addition, users of Synplify Premier need not synthesize and floorplan their designs if their designs consist entirely of synthesizable RTL code. Users can feed the tool RTL code, push a button, and watch the tool find the optimum floorplan, placement, and routing. The tool concurrently performs synthesis, floorplanning, placement, and prerouting, and the vendor's proprietary router performs detailed routing. However, designers who are using a hard or firm macro or who want to tweak the layout must buy the DesignPlanner floorplanner add-on, which costs $15,000 to $29,000 more than the $34,000 to $74,000 cost of Synplify Premier.

The top-of-the-line version of Premier also features a built-in version of Synplicity's Identify debugging engine and a scaled-down version of the company's Certify ASIC-prototyping tool. The scaled-down prototyping technology allows users to create ASIC prototypes on a single FPGA. This creation includes most FPGA-prototyping projects, according to Garrison, because many users employ a single FPGA to test new functions they plan to add to a design they previously implemented in an ASIC. Users will need full-blown Certify if they want to prototype ASIC designs in more than one FPGA.—**by Michael Santarini**

▷**Synplicity**, www.synplicity.com.

FEEDBACK LOOP

"Our children ... all want to be high-flying lawyers, CEOs, VPs ... They want to drive BMWs, drink lattes, and live in $1 million homes. Can't do that by learning op amps and writing embedded code!"

"F. Ed Upp," in *EDN*'s Feedback Loop, at www.edn.com/article/CA6280033. Add your comments.

DILBERT *By Scott Adams*

Embedded video card drives multiple displays

12.16.05

With security, medical, transportation, industrial, and aerospace applications in mind, VersaLogic recently announced a PC/104-Plus video module. The EPM-VID-3 supports embedded-system applications with 24-bit color and resolutions as high as 1600×1200 pixels. The module supports a wide range of display types, including CRT displays, LVDS flat panels, and NTSC video monitors. Key features include an 8-Mbyte video RAM, the ability to simultaneously output as many as three displays, and hardware-based MPEG-2 decoding.

The module also boasts low power consumption, a customizable video BIOS, and TV output for NTSC-type monitors. The EPM-VID-3 can operate as a primary or a secondary video device or as a temporary video output during PC/104-Plus system development and testing. The EPM-VID-3 is available now and sells for $237 (OEM quantities).

—**by Warren Webb**

▶**VersaLogic Corp**, www.versalogic.com.

Featuring the ATI Rage Mobility M1 graphics controller, the EPM-VID-3 video card offers high-performance video output for embedded-system applications.

14-Bit, 190 MSPS ADC

Speed and Performance

Device	Resolution	Speed	SNR	SFDR
ADS5546	14 Bits	190 MSPS	73.2 dBFS at 70 MHz IF	84 dBc at 70 MHz IF
ADS5545	14 Bits	170 MSPS	73.5 dBFS at 70 MHz IF	85 dBc at 70 MHz IF
ADS5444	13 Bits	250 MSPS	68.6 dBFS at 230 MHz IF	78 dBc at 230 MHz IF
ADS5440	13 Bits	210 MSPS	69.1 dBFS at 230 MHz IF	79 dBc at 230 MHz IF

The new high-performance, low-power ADS5546 ADC from Texas Instruments features 1.1W total power consumption in an ultra-small, 7mm x 7mm QFN package. It supports both high SNR and SFDR at high input frequencies and offers unprecedented interface flexibility with user-selectable CMOS or DDR LVDS outputs. The ADS5546 is ideal for demanding applications such as wireless communications, video, imaging, instrumentation, test and measurement.

High Performance. Analog. Texas Instruments.

For datasheets, samples and evaluation modules, visit
www.ti.com/ads5546

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Generator produces precise digital waveforms to 13.5 GHz

Agilent has announced a serial pulse/data generator with stimulus capability to 13.5 GHz. The Agilent 81142A, which—except for speed—is similar to a 7-GHz generator that the company announced less than a year ago, enables reliable physical-layer measurements for high-speed serial-bus designs.

Next-generation computing and communication applications, such as video on demand, require transferring large amounts of data at greater rates. Obtaining high-quality characterization of electronic-component performance is a key step in designing reliable, high-performance systems. In addition, researchers are now developing next-generation electrical components to operate at speeds of 10 GHz or more; currently, such speeds usually require optical communication. Accurate high-speed stimuli are crucial to ensuring signal integrity at these speeds. By providing high-precision, low-jitter signals and permitting full control of data streams for performance and characterization testing, the Agilent 81142A allows engineers to conduct reliable, accurate physical-layer tests.

"Accelerated development cycles make proprietary test approaches less suitable," says Siegfried Gross, vice president and general manager of Agilent's Digital Verification Solutions Division. "Standard test instruments that do not compromise on signal quality, timing accuracy, or programmatic control give engineers a jump-start in high-quality characterization of new devices and systems," he says. Agilent asserts that the device's combination of multiple data formats with sequencing, flexible triggering, and 13.5-GHz performance is unique in the market.

Superior signal fidelity and the most precise data signals are the key contributions of the 13.5-GHz serial-pulse/data generator. Other features include: RZ (return-to-zero), R1 (return-to-one), and NRZ (non-return-to-zero) data formats; flexible parameters and fast transition times for high-quality waveforms and eye-diagram measurements; flexible and programmable pattern and sequence generation for high-speed serial digital buses; linear-delay modulation to 1 GHz for jitter-tolerance testing; and remotely programmable, ultrasmall pulses to trigger accurate measurements. The 81142A is available now for $108,000.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/High_Speed_Pulse.

The 81142A generator produces high-quality pulse trains to 13.5 GHz.

ARM7 cores target FPGA users

12.16.05

Actel's microprocessor-core-licensing deal with ARM (www.arm.com) has come to fruition with the announcement that Actel customers can now license a firm, Actel-architecture version of the 32-bit ARM7 TDMI-S core directly from Actel. ARM and Actel this year announced their licensing deal, and ARM officials say that they chose Actel over other vendors largely because Actel's flash-based devices offer better IP (intellectual-property) protection than competing offerings. In the past, ARM has jealously guarded its IP, mainly offering direct licensing. But Actel customers can now get the core directly from Actel without negotiating with ARM. "People wanting to put a processor into an FPGA didn't have many choices—or, certainly, a popular choice such as the ARM7, which is likely the most used and well-known 32-bit core," says Dennis Kish, vice president of marketing at Actel.

The Actel version of the ARM core, CoreMP7, is a firm, rather than soft, core, such as Verilog or VHDL source code. The companies chose a firm core in part to ensure that the core maintains 25-MHz performance in Actel devices and in part to ensure no one can tamper with or steal the core. The core appears as a black box during the synthesis of the design, but users can adjust the bus interface and peripherals and have full control of the I/O, according to the company. To ease configuration of the core's peripherals, Actel offers the new CoreConsole tool.

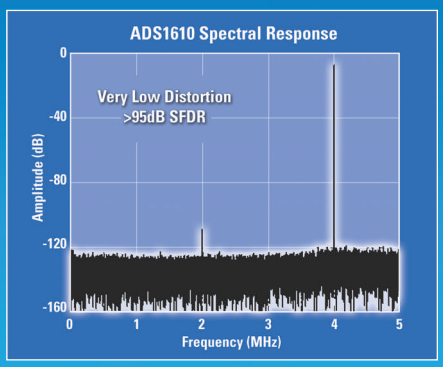
The Windows-based tool allows users to configure the processor's peripherals, including interrupt controllers, memory controllers, timers, serial interfaces, I/O ports, and power-on-reset circuitry. The tool also has a repository of other Actel cores and complies with the SPIRIT (Structure for Packaging, Integrating and Reusing IP within Tool flows) standard. For those familiar with ARM's RealView development-tool suite, Actel also offers an Actel-specific version of RealView. The core consumes roughly 6000 ProASIC tiles or roughly 250,000 system gates. Actel provides the core free to customers buying ARM-ready M7 ProASIC3 devices; the M7A3P250, M7A3PE600, and M7A3P1000 devices are available for sampling now. The company expects to offer the core with other FPGA families, as well.**—by Michael Santarini**

▶**Actel**, www.actel.com.

16-Bit, 10MSPS ΔΣ ADC

Speed with Precision

Featuring 86dB signal-to-noise ratio over a 5MHz signal bandwidth, the ADS1610 data converter provides state-of-the-art performance at 4x the speed of the nearest competition. This unmatched combination of speed and precision extends TI's portfolio of high-speed delta-sigma converters for demanding measurements in communications, scientific instrumentation and test & measurement applications.



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www.ti.com/ads1610

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Texas Instruments

POL power modules boast fast transient response

Power systems for networking and communications systems must respond to the transient-power needs of powerful system processors, such as DSPs, FPGAs, ASICs, and microprocessors. To fulfill that need, Texas Instruments' new T2 series of POL (point-of-load) dc/dc-converter modules incorporates TurboTrans, a feature that allows designers to customize the modules for specific transient-load requirements. "TurboTrans allows you to tune the feedback loop so that you get the maximum amount of transient response from the module, which allows you to reduce the amount of capacitance that you have on the output to respond to the transients," says Don Matthiesen, marketing manager for TI's power-management product line. The end result is faster transient response with 40% less output-voltage deviation and a five- to eight-times reduction in output capacitance.

"Some IC manufacturers have reduced the overall tolerance on the core-voltage rail from 5% to 3%," he says. "These are typically 1 or 1.2V rails, so when you start talking about 3% of a 1V rail, only 30 mV can let that voltage rail swing under transients. So, designers have to pay attention to how much of a transient they have and make sure that the core-voltage rail stays within the specification."

The modules also incorporate the SmartSync function, which allows designers to synchronize the switching frequencies of multiple T2 devices, maximizing power efficiency and minimizing EMI. SmartSync also allows the T2 modules to synchronize at different phase angles using external circuits to help balance source loading and minimize input capacitance. The synchronized modules also ease EMI filtering by eliminating beat frequencies. The series supports step-down dc/dc conversion from a 4.5 to 14V input, with adjustable output voltages as low as 0.7V at output currents to 50A, which is useful for IBA (intermediate-bus-architecture) applications. The power modules reduce the overall power footprint by as much as 50% compared with TI's previous-generation devices, according to the company.

T2 power modules are available now in sample quantities. Prices begin at $7.90 (1000). Evaluation modules of the T2 family, application notes, and TI's online selection tool for power-management products are also available at www.power.ti.com.

—by Margery Conner

▷**Texas Instruments**, www.ti.com.

FEEDBACK LOOP

"The very environment that causes folks to find *Dilbert* funny or apropos is the very reason that more students don't go into science or technology."

Daryl P Dacko, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6280033. Add your comments.

Vendor triples power available from compact dc-supply system

By introducing four new modules and two mainframes, Agilent has extended the output capability of its N6700 MPS (modular-power system) to 1200W. Company officials claim that Agilent is now the industry leader in the number of outputs and amount of power that a 1U (1-75-in.-high), rack-mountable, programmable dc-power system can provide.

According to a spokesman, these products represent the next step in a series of enhancements that give test-system integrators the flexibility to optimize performance, power, and price to match test needs in such industries as aerospace/defense, consumer electronics, computers and peripherals, communications, semiconductors, and automotive.

"Our customers value the size, mix-and-match design, and performance of the N6700," says Scott Sampl, vice president and general manager of Agilent's System Products Division. "They have asked for more power in the same small, flexible, and fast package, and we've given it to them. And more enhancements are on the way."

Offering 600 and 1200W capabilities, the two new mainframes join the currently available 400W mainframe. All mainframes accommodate one to four modules in a system-ready, 1U package. Four new one-slot-wide, 300W basic programmable-power-supply modules extend the system's range of outputs to 20V at 15A and 100V at 3A.

The four new modules, together with the 16 others, constitute a family ranging in power from 50 to 300W at basic-, high-, and precision-performance levels. Test-system integrators can mix and match any of the 20 modules in any of the three mainframes to create dc-power systems that provide one to four outputs totaling 400, 600, or 1200W at prices from $1000 per output.

The N6702A 1200W mainframe automatically senses power available from the ac line and scales back the available output power accordingly, allowing you to plug the high-power mainframe into any standard outlet.

New power-management features allow users to allocate mainframe power to the outputs where it's needed. According to Agilent, this feature is unique in the market and prevents unexpected and dangerous shutdowns that can occur when you attempt this type of operation with power systems that lack power-management features.

The 1200W N6702A mainframe automatically senses power available from the ac line and scales back the available output power accordingly, allowing you to plug the high-power mainframe into any standard outlet. The system-ready N6700 test instruments comply with LXI (LAN extensions for instrumentation) Class C. They provide USB 2.0, 10/100 BaseT Ethernet (LAN), and IEEE 488 interfaces as standard features. You can also operate the units remotely from any browser you connect to a unit's built-in Web page. A free download upgrades older N6700 mainframes to support the new modules and to provide the power-management capability.**—by Dan Strassberg**

▶**Agilent Technologies**, www.agilent.com/find/n6700_backgrounder.

Outstanding RF performance—at outstanding prices.
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New log amps extend RF power measurement to 10 GHz

ADI's new log amps redefine the parameters of accurate RF power detection. These detectors support all cellular and broadband wireless standards and other demanding applications up to 10 GHz—enabling designers to address more applications with less time and effort. They also provide performance and value that are unsurpassed in the industry.

From RF to IF, mixers to power detection, for handsets to base stations—analog is everywhere.

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- Better than ±0.5 dB stability over temperature
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- Pricing: $3.93/1k USD

AD8318
- Operating 1 MHz to 8 GHz
- 60 dB dynamic range
- Better than ±0.5 dB stability over temperature
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- Operating 1 MHz to 10 GHz
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ANALOG DEVICES

VOICES

Intel's Ron Resnick:

wearing two hats

When it comes to multitasking, few people could beat Ron Resnick. He divides his time between working at his "day job" as Intel's director of marketing for its broadband-wireless division and serving as president and chairman of the WiMax Forum, an industry concern dedicated to the open interoperability of products for broadband-wireless access. In his role at the WiMax Forum, he oversees strategic and tactical operations involving the emerging wireless-broadband technology.

What is the current state of WiMax technology? Are things on track?

A Things are definitely on track on the chipset side. First-generation WiMax chips are out there now; companies started to ship them in volume six months ago. The technology is starting to mature, too. Big companies, such as Fujitsu and Intel, have jumped into the mix, as have smaller players from the fixed domain of wireless access, such as Alvarion, Aperto, Wi-LAN, and Redline. We are in the position where the first-generation of mature 802.16-2004 silicon is out there in the market. And products based on that silicon, particularly on the client side, are going out in volume, with the 802.16e silicon for mobile-broadband development about to begin.

What are the biggest challenges in mass deployment and implementation of WiMax-based technologies for semiconductor and CPE (customer-premises-equipment) vendors?

A The one thing that did not get accomplished in the 3G world: to have one technology that delivers on a global platform. With 3G, there have been at least five iterations, such as EV-DO, WCDMA, HDSPA, HSUPA [evolution-data only, wideband-code-division multiple access, high-definition single point of access, high-speed uplink-packet access], and so on. The things we are trying to do with WiMax, at least when we get to 802.16e, is to jump-start it, prove that it works, and prove that there is a need for fixed broadband in many areas where you can't spend the money to do wire line, such as in parts of India and China, where the wireless infrastructure represents less than 10% of telecom. Why are they going to run wires for broadband when they don't even have phones or wire lines? The way to do it is wireless, and broadband and fixed wireless is a big market segment. With 802.16e, the plan is to deliver personal broadband experiences, and I think that scenario is going to happen.

What do engineers need to know when they go about their design work to implement a system or work on a WiMax-centric platform?

> "Why are they going to run wires for broadband when they don't even have phones or wire lines?

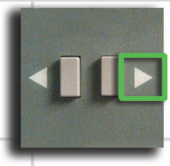
A Because WiMax requires the use of a fair amount of design tools, we need a better way to develop design tools to accelerate the development of new chip sets for broadband silicon and perhaps telecom silicon. It is important to look at the processes in use, such as CMOS and SiGe [silicon-germanium], and which ones are going to give the best performance for long-term development. Because design tools are so complex in nature to begin with, maybe there is a way to automate the design process and make it incorporate building blocks.

There has been a lot of talk about a perceived engineering shortage in the United States. What needs to be done to bump up the numbers and get things moving in the right direction?

A This problem has become a common one in the United States, and one reason is poor education. Middle and high schools are not doing enough to develop interest in engineering. Part of the reason is that we are not doing enough to generate interest because the curriculums are lagging. There is virtually no computer and technology training at this level, and science is minimal. There is now a push to improve this situation, but it remains a serious problem. We need to establish funding and develop a national education program that works, because we are getting killed. And if this shortage continues, the United States will be second to other countries, because they are working harder on education and developing engineering talent.

—by Jeff Berman,
Contributing Editor

Amplifiers to ADCs, Shanghai to San Jose, analog is everywhere.



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Trendy phones incorporate sophisticated engineering

Both the Rokr (left) and Razr (right) mobile phones incorporate Freescale Semiconductor's dual-core DSP56631 baseband processor and the quad-band MC13777 GPRS front-end ICs.

With their ultraslim form factors and cool looks, Motorola's Razr and Rokr mobile phones have helped transform Motorola's image from an engineering-focused company to a hip, trend-setting, marketing company. But few know about the company's connection with India. Both phones incorporate Freescale Semiconductor's dual-core DSP56631 baseband processor and the quad-band MC13777 GPRS (general-packet-radio-service) front-end ICs—chips that Motorola designed at its Bangalore development center.

The Indian designers were involved in the development, verification, and validation of the phones' baseband chip—a dual-core IC comprising multiple IP (intellectual-property) blocks. According to Freescale, This SOC (system-on-chip) design was the first to integrate the analog part of the RF into the baseband to reduce the overall cost of the chip set. The baseband processor integrates a Freescale DSP-56600 DSP with an ARM7-TDMI-S microcontroller. Functions include on-chip memory, receiver ADCs, a receive-and-transmit synthesizer, transmit power-amplifier control, and a voice codec. The front end works in GSM/DCS (Global System for Mobile communications/Digital Communications Services) and GSM850/PCS (personal-communications-services) quad-band GPRS Class 10 cellular radios. It has a receiver portion that works in VLIF (very-low-intermediate-frequency) receivers and DCRs (direct-conversion receivers).

To meet Motorola's performance and cost constraints, Freescale engineers integrated analog-baseband capability with the digital baseband in a high-speed SiGe (silicon-germanium) process. They also built low-noise amplifiers into the RF transceiver to support all four GSM bands—making the chip set smaller without sacrificing performance. One of the more difficult problems confronting the designers was deciding where to put the analog functions for both the RF chain and the audio portion. Freescale designers integrated power-management and audio features into a single chip, thereby eliminating noise-related issues and conserving space.

On the software front, Motorola's Indian development center worked on the phone's multimedia features, such as image and video capture, multimedia messaging, the user interface, the phone browser, and the GSM-signaling stacks.

—by Chitra Giridhar, *EDN Asia*

▷**Motorola**, www.motorola.com.

▷**Freescale**, www.freescale.com.

Poland moves into technology

12.16.05

With its recent transition from the Soviet Block to the European Union, Poland now has the opportunity to make its mark on the world. President Lech Kaczynski has promised government support for high-tech companies and a more commercially favorable administration. One area in which the country can raise its position in the semiconductor hierarchy is programmable logic. With FPGAs' gate density increasing, operating speeds increasing, and voltages decreasing, signal integrity becomes a serious concern. Debugging tools that FPGA vendors supply and proprietary software packages are no longer enough. Aldec-ADT (Katowice, Poland) manufactures software for enhanced verification. Its Active-HDL integrated environment for designs in VHDL and SystemC uncovers glitches and pinpoints sections of code that these glitches relate to, allowing the rapid performance of alterations.

Another Polish company, Microtech, got its start in the early 1990s, aiming to develop hardware and software for signal-processing systems in radar. The highly reliable products it now produces match military/aerospace requirements. Resistance to harsh conditions, strong processing power, automatic testing and fault diagnosis, and advanced programming techniques bring benefits to such designs. The products use IP (intellectual-property) core technology to link hardware, algorithms, and software within FPGAs, resulting in faster, more flexible systems. A portfolio of demo boards based on Spartan II devices gives designers a platform on which to perform ASIC prototyping and test implementation.

Evatronix (Gliwice, Poland), which is a spin-off of the Silesian University of Technology, specializes in soft cores that enable engineers to cut time to market for SOC (system-on-chip) designs. The company supplies the cores with VHDL or Verilog-HDL source code or as postsynthesis netlists. Firm versions of cores for both Altera and Xilinx devices are available, allowing quicker turnaround times.—by Mike Green, *Electronic Product News*

▶**Aldec-ADT**, www.aldec.com/pl.

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Agilent Technologies

BY BONNIE BAKER

The power of moving-average digital filters

Many times, ADC users employ averaging algorithms with their controller or processor on the output of several samples from the converter. You can "smooth" a converted signal using this technique (**Figure 1**), as well as improve the effective resolution of the system by reducing system noise.

You implement the smoothing effect on your converted data by acquiring multiple signals at a constant sample rate, averaging a predetermined group or number of samples, and then continuing this process with several groups over time. As **Figure 1** shows, the aggregate of the averaged results produces a smoothed signal. This averaging technique essentially provides a lowpass filter on the converter output data. You can control the effectiveness of your filtering by selecting the appropriate number of samples for the averaged groups. If you use more samples in each group, you will see a higher degree of smoothing. This averaging process eliminates spikes in the raw data as well as reduces the bandwidth of the final signal.

Another by-product of this averaging technique is that the conversion resolution or precision of the data increases. Ideally, an average of four samples (4^1) of a dc signal will increase the converter's effective resolution by one—a 6-dB increase in the SNR (signal-to-noise ratio). An average of 16 samples (4^2) will increase your resolution by two and your SNR by 12 dB. Theoretically, a group size of 4^N will increase the number of effective bits from your conversion by N, but there are real-world limitations to this theory.

It is possible to increase the number of effective bits with your ADC, as long as you maintain realistic goals and consider nonideal conditions. For instance, improving a 12-bit converted result to 16 bits requires 4^4 samples for averaging. Four to the fourth is equivalent to 256. The first question you should ask is, "Do I have time to implement the required algorithm in my controller or processor?" If you are trying to achieve a higher resolution than 16, the required sample size increases very quickly. By the way, the lower bits of the 12-bit converter in this discussion should be noisy so that the averaging is effective. This noise should be Gaussian.

Nonideal conditions that can affect the size of your averaging group include drift of the input over time, power-supply variations, voltage-reference changes, and temperature effects on your system. Any of these nonideal conditions can change the output value of your conversion. The sample size for a nonideal system can change from 2000 (with an ideal driftless system) to several hundred samples. If you increase the sample size above a few hundred samples for this nonideal system, the results begin to get noisier again. However, you can use Allan variance methods to compute the optimum number of averages for your data set. Finally, examine your input signal and ensure that you are not trying to convert an analog signal that has a settling-time error or an interfering periodic signal, such as the mains frequency.

There are time-saving ways of implementing averaging algorithms that go beyond the simple, brute-force technique of collecting all of the data and then performing an average. For instance, you could implement a FIFO by adding a new data point and subtracting the first data point accumulated in the group. Additionally, you can select the size of the groups to enable the use of a shift right for the division of the total, such as group values of 4, 8, 16, and so on. EDN

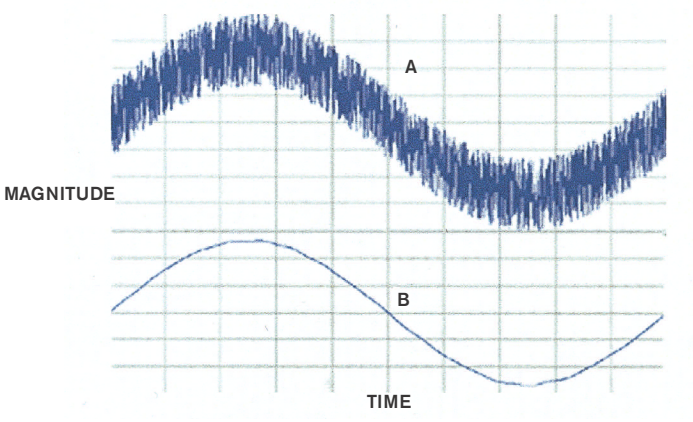

Figure 1 You can smooth an ac signal that has small signal noise riding on top of it (A) by employing an averaging filter to a large number of consecutive samples (B).

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Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.baker@microchip.com.*

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Go to www.edn.com/051216pe to see images of the meat of the Mac Mini as well as a more detailed write-up.

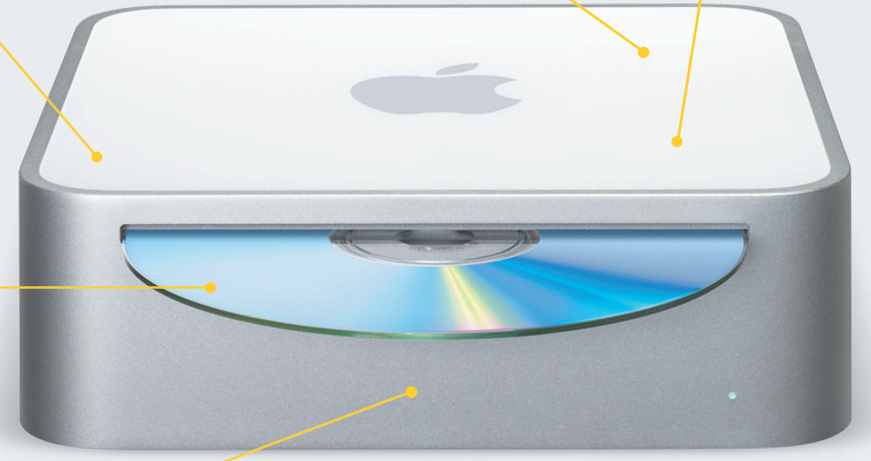
Thinking different

With the Mac Mini, Apple squeezes substantial computing horsepower into a diminutive form factor

The carefully thought-out design of the Mac Mini enables Apple to squeeze a solid-performing, quiet, and cost-effective computer into a 6.5×6.5×2-in., less-than-3-lb form factor. Read about some of its elements here, then visit www.edn.com/051216pe for a more in-depth description of the Mac Mini's building blocks, along with a series of high-resolution images of the system internals, courtesy of Other World Computing (www.otherworldcomputing.com).

Rectangular antennas for the Mac Mini's Bluetooth/WiFi wireless module clip to the internal frame at the top of the unit; the Bluetooth antenna is in the front left corner, and the WiFi antenna is in the back right corner. Along the left side of the system is the single-slot PC7200 (DDR-266) DRAM module.

Wireless mezzanine and analog modem boards mate to the main system board by means of connectors and mounting screws. Underneath a passive heat sink, you'll find the Freescale G4 PowerPC CPU, along with ATI Technologies' Radeon 9200 graphics processor and its corresponding 32 Mbytes (64 Mbytes on latest generation systems) of frame-buffer DRAM.



A Matsushita/Panasonic UJ-835F SuperDrive plays and burns DVDs (as well as CDs); lower priced system variants contain "Combo Drives" capable of only reading DVDs (but still able to both read and write CDs).

Underneath the optical drive is the 2.5-in. hard-disk drive. When swapping out the drive for a faster replacement, a denser one, or both, be careful to note that it's mechanically possible to install the hard-disk drive upside-down!

Airflow is one of the most intriguing aspects of the system design. Air enters the system through a series of vents at the periphery of the Mac Mini's underside. It flows through a fan and over a passive heat sink and finally exits the system through a vent at the back of the unit, where you'll also find two USB2 connectors, a Firewire-400 connector, a DVI-I video port, a 10/100-Mbit Ethernet port, a modem port, a headphone jack, a power connector, and the on-off switch.

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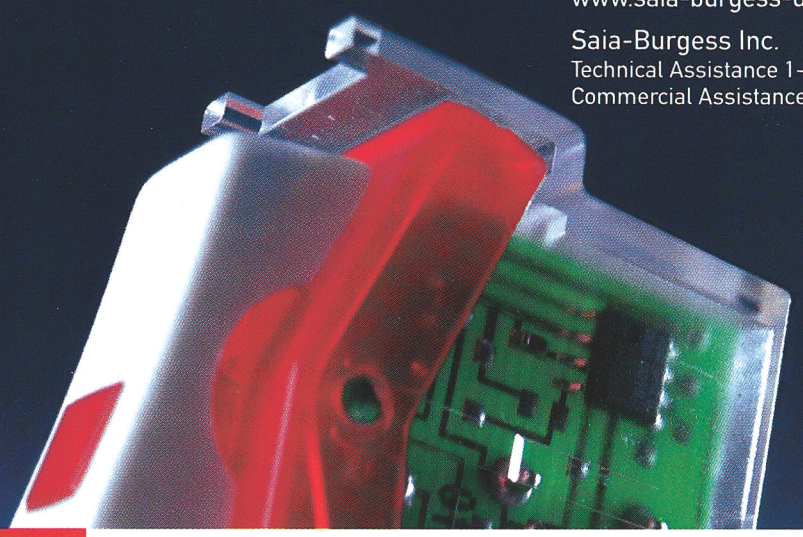

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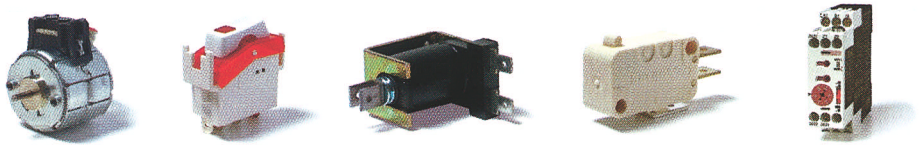

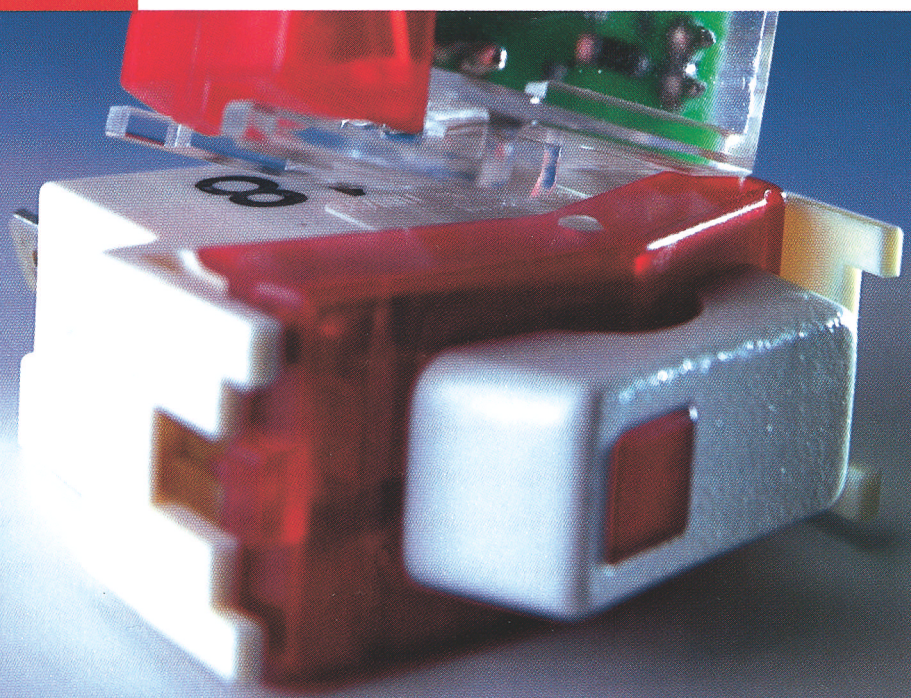

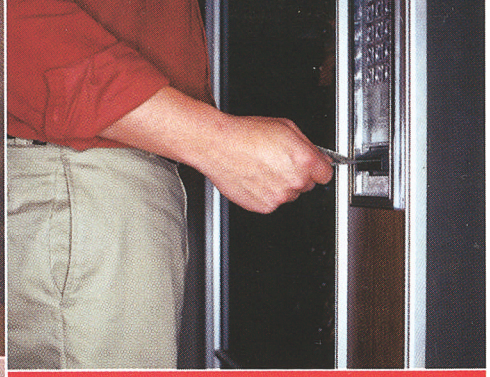

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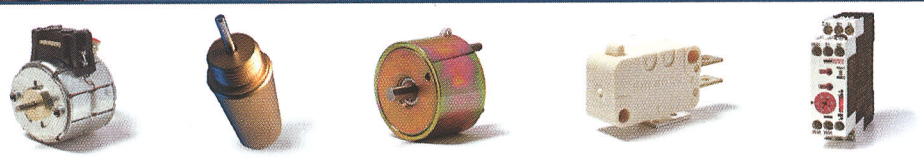

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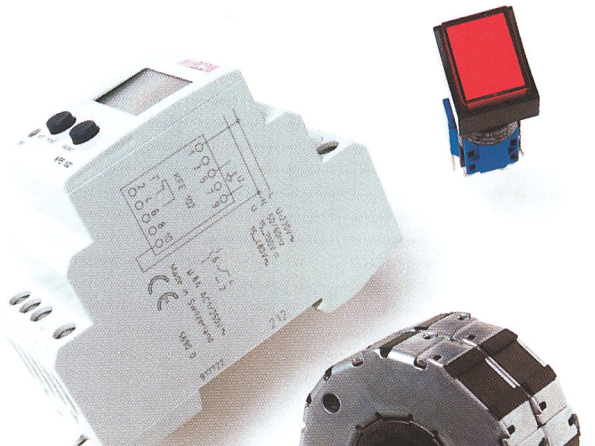

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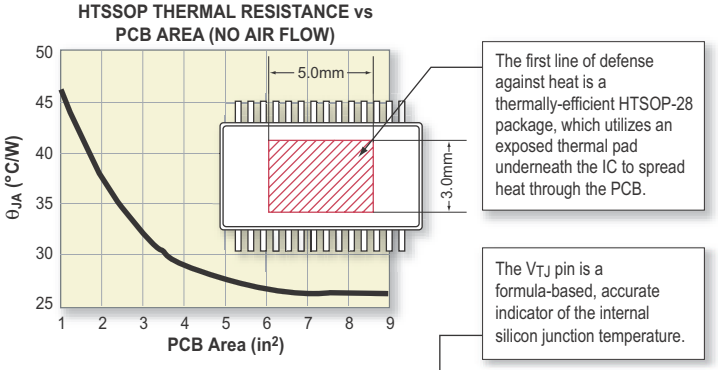

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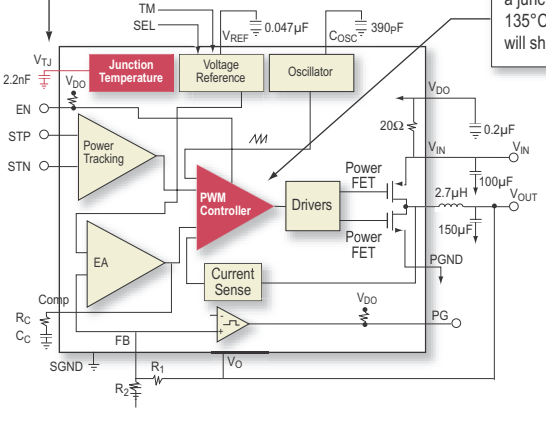

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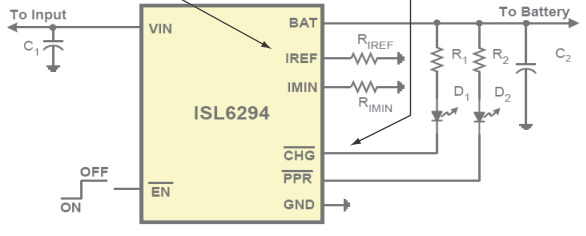
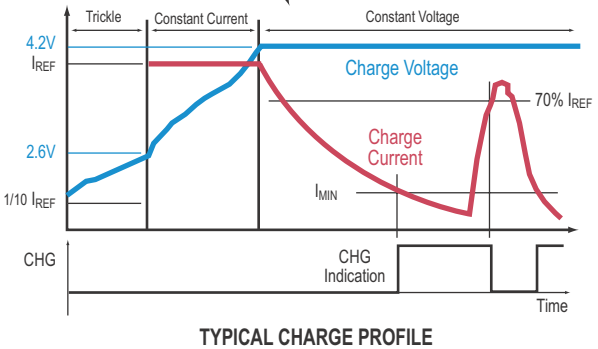
End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



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HOT 100 PRODUCTS OF 2005

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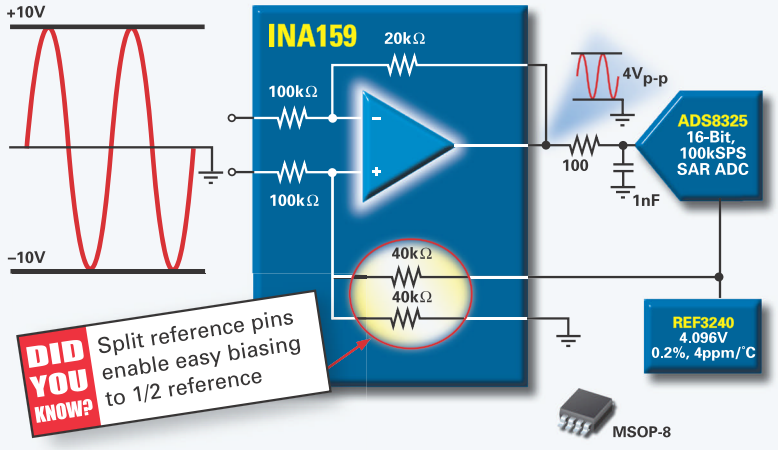

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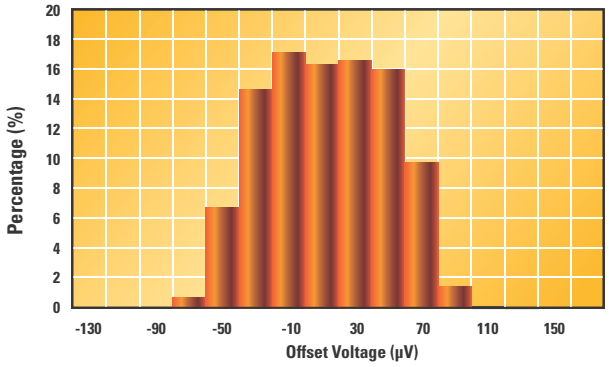
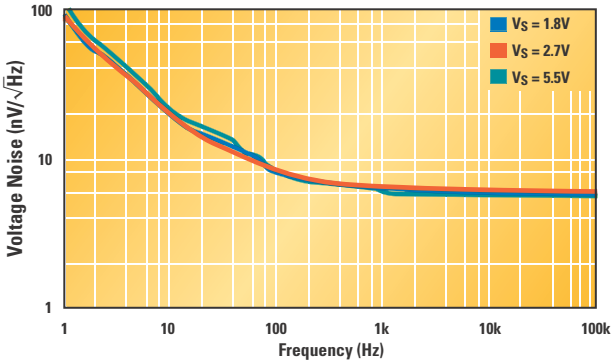


LMP7711 Input Voltage Noise vs Frequency



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LMP7701	Precision, 12V RRI/O CMOS	0.73	2.7 to 12	0.2	2.5	✔	-40 to +125
LMV651	90% Power Saving RR/O Performance Amp	0.11	2.7 to 5.5	1.0	12	—	-40 to +125
LMV791	Low-Noise, Low I_{BIAS} RR/O	0.95	1.8 to 5.5	1.3	14	✔	-40 to +125
LPV511	880nA, Ultra Low Power 12V RRI/O	880 nA	2.7 to 12	3.0	0.027	—	-40 to +85

Comparators

Product ID	Key Features	Typical Supply Current (nA)	Supply Voltage Range (V)	Input Offset Voltage (mV) max	Prop Delay Time (µs)	Low Input Current CMOS Design	Temp Range (°C)
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QUANTUM CRYPTOGRAPHY:

WHEN YOUR LINK HAS TO BE REALLY, REALLY SECURE

COMBINING QUANTUM THEORY AND SINGLE PHOTONS, SYSTEMS CAN ACHIEVE SECURITY THAT THE LAWS OF PHYSICS—RATHER THAN AN ALGORITHM'S COMPLEXITY—ASSURE.

Keeping data and communications secure is a hot topic. Hackers access systems through open ports, through secret programs, and through various ruses or aliases. As a result, data-security products and strategies are top priorities for both embedded and enterprise systems.

Another long-recognized weakness in any system is the physical link that connects users or system nodes. Although several ways, such as a private channel or a physically secured link, exist to minimize this risk, it is more common to use data encoded using a complex, mathematics-based approach, such as the RSA (Rivest/Shamir/Adleman) algorithm or a one-time key. Physically securing the link is often impractical and rules out wireless links; data encoding is susceptible to decoding by a determined eavesdropper. (Even the RSA algorithm may face this challenge as computers get more powerful.) And the one-time key, although absolutely secure in principle, has severe implementation problems in practice (see **sidebar** "Encryption basics" at the Web version of this article at www.edn.com/051216df1).

But a technique now in use appears to offer

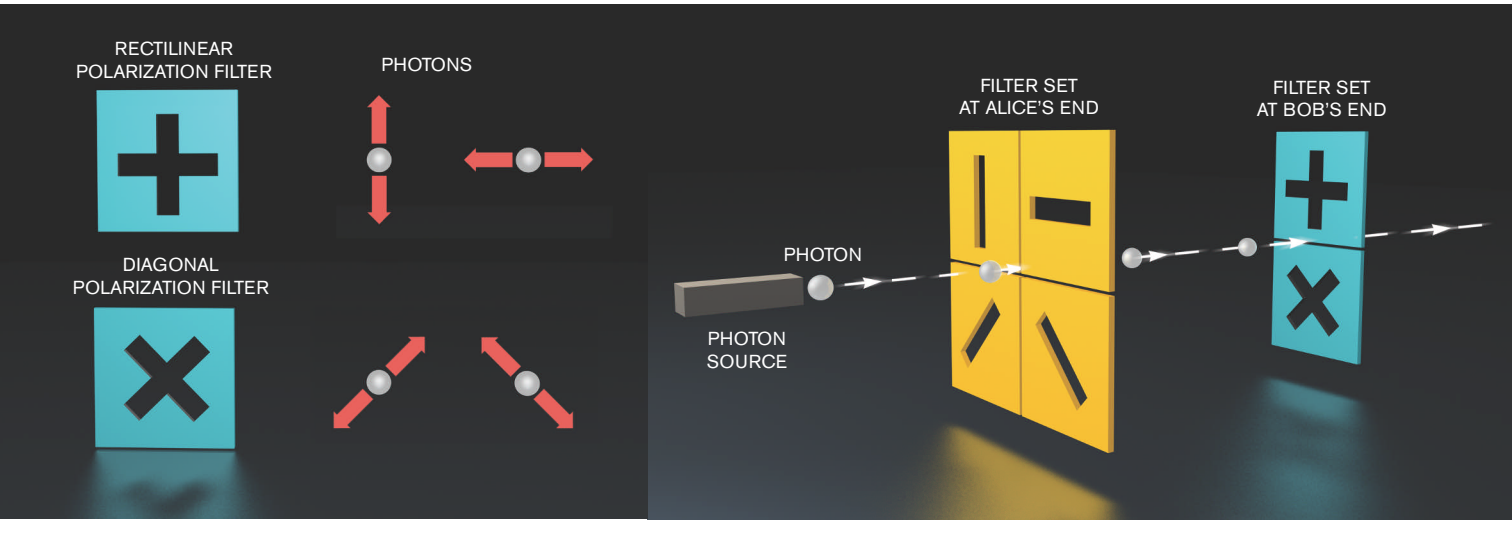


Figure 1 BBN and DARPA based the QC system on the random polarization of photons, followed by selective polarization filtering and polarization-direction detection.

AT A GLANCE

- QC (quantum cryptography) promises absolute data-link security, based on the laws of physics, photon quantum states, and the uncertainty principle.
- A multimode QC system has been running for more than two years, linking three Boston-area institutions through standard dark fiber.
- You can use the QC system for either one-time-pad or key-passing modes of cryptography.

the security of the one-time key without its key-management problems, and you can also use it for absolutely secure key exchange. QC (quantum cryptography) uses a string of individual photons and their quantum states as the bases of a link in which physicist Werner Heisenberg's often-cited, often-misunderstood uncertainty principle defeats any eavesdropper (**Reference 1**). Although IBM corporate researcher Charles Bennett and the University of Montreal's Giles Brassard first conceived quantum cryptography in the 1980s, it took many years for the needed optical components and associated technologies with the required performance to become available.

A fully operational QC system has been running in the Boston area since June 2004 over a 12-mile loop and with 10 nodes. BBN Technologies (www.bbn.com) developed the system with the cooperation of other labs and companies under a 2002 DARPA (Defense Advanced Research Projects Agency) grant. BBN, an R&D facility, aims to license the technology to others for commercialization. Although the system is not in regular commercial deployment, it is more than an academic proposal or lab curiosity: It runs 24 hours a day, seven days a week; is fully operational; and requires virtually no intervention to keep it going.

The QC system also includes an Internet gateway, so that its users can reach out and link beyond the QC-encrypted nodes, although they lose the QC once they cross the gateway. BBN has a long history of research and development in communications and networks; in the late 1960s, the company—then better known as Bolt Beranek and Newman—led development of and launched the ARPAnet (Advanced Research Projects Agency network), the underlying structure of the Internet. BBN has the perspective of a telecom and networking organization, not an experimental-physics lab; it seeks to develop systems with near-100% uptime rather than "prima donna" operations that require constant care, attention, and restarts.

Vendors such as id Quantique (www.idquantique.com), MagiQ Technologies (www.magiqtech.com), and QinetiQ Ltd (www.qinetiq.com), offer commercially available QC products and subsystems.

QUANTUM IDEAS: NOT INTUITIVE

Before discussing how a QC system works, it's a good idea to review the quantum principles and orient yourself with some "out-of-the-box" thinking, compared with conventional signals, power, and observations (see **sidebar** "Think differently"). A QC system starts with a source of single photons and a pair of polarizing filters (**Figure 1**). (How you generate these photons is not trivial. One polarizing filter—the rectilinear filter—allows only photons having vertical or horizontal polarization to pass. The other filter—the diagonal-polarizing filter—allows only photons with polarization that is oriented at ±45° to the horizontal or vertical to pass. The frame of reference is arbitrary; just define one direction as the horizontal and use it as the baseline orientation for subsequent angles.)

For each photon that the source generates, the sender, which the relevant literature typically calls Alice, randomly passes it through either the rectilinear or the diagonal filter. If she uses the rectilinear filter, Alice records whether the photon that passes has horizontal or vertical polarization; if she uses the diagonal filter, she records whether the photon's polarization is tilted right 45° or left −45°. The photon, representing a bit of data, then travels through an optical fiber or free space.

At the receiving end, the receiver, which the relevant literature typically calls Bob, makes a random choice of whether to observe the incoming photon with a rectilinear or a diagonal filter, and he notes the filter he uses and the polarization value he sees—horizontal or vertical, 45° or −45°. This number is his bit value. He repeats this procedure for all incoming photons. Bob then contacts Alice over an open, nonsecure channel and tells her the sequence of filters he used. He does not tell her the bit values, or "qubits," he recorded using this sequence.

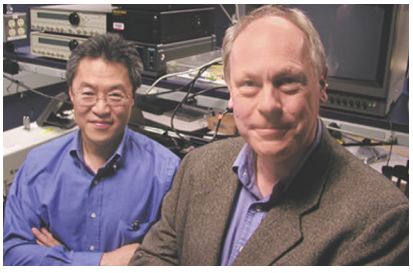


Figure 2 Henry Yeh (left) and Chip Elliott of BBN Technologies have led the DARPA-funded quantum-cryptography project.

Alice responds to Bob, again over an open channel, and tells him which of the filter orientations he used were correct. She doesn't comment on the bit values, because he has not given them to her. Alice and Bob use the instances in which the modes were correct as the key to encrypting and decrypting messages and ignore the positions in which the photons were not seen in the right mode.

What about the ever-hovering potential eavesdropper, which the relevant literature typically refers to as Eve? Due to the Heisenberg principle, she can't simultaneously measure the photons in both the rectilinear and the diagonal modes. Further, if Eve guesses, makes the measurements in the wrong mode, and resends the bits to Bob the way she measured them, she will introduce errors. Both Alice and Bob will detect the eavesdropper just by comparing selected bits and doing some error checking on their bit pairings.

The QC technique meets the needs of a secure link. You can use it either for sending a secure key from Alice to Bob or for creating and sending a one-time key along with the message bits. But it has limitations. First, it works over the distance of only a single, uninterrupted link, because any all-optical or electro-optical repeater or amplifier for the photons destroys their quantum states; no currently available opti-

cal-repeater design also preserves those states. A QC link employing the standard, low-loss fiber used for telecom can reach through about 100 km of fiber, and the free-space link with a carefully focused telescope at the receiver end achieves 20 km at night. (Daytime use is difficult due to the brightness of the sun.) Researchers believe that a link from a low-orbit satellite to a ground station is possible with suitable optical components, however.

Second, the data rate is relatively low, due to limitations of some of the optical components and the protocol complexity. When you use QC for sending a secure key, the link achieves rates of about 5 Mbps; when you use it for a one-time key, the system sends key material at 700 bps.

ONE PHOTON TO GO, PLEASE

Implementing a working QC system requires many functional blocks and pieces of equipment. Many are standard items; a few are not. Chip Elliott, principal engineer at BBN, and Henry Yeh, program manager, along with others did much of the work (**Figure 2**).

The system currently has nodes at BBN, Harvard University, and Boston University's Photonics Center, over a 12-mile loop of unused, commercial, dark optical fiber that is already in place. BBN, along with engineers at the NIST (National Institute of Standards and Technology, www.nist.gov), also developed a free-space link from BBN to an adjacent building (**Figure 3**). The system is not just a simple point-to-point, single-protocol topology; it has electro-optical repeaters at each node to capture, recover, re-encrypt, and retransmit the data using QC, and it uses different data protocols.

A single-photon source and the corresponding single-photon detector are critical to a QC system. BBN's system has two methods of generating the single photons: One technique uses a laser and filters its output, and the other is an entangled-photon approach. In the first method, a filter drastically attenuates the output of a laser, or a phase-modulation path acts as the filter and separates the photons. This filtered-laser approach is the simpler of the two methods, in principle, but it is hard to precisely filter down to one photon. The attenuated, filtered output may comprise one, two, or even three photons, because, in the quantum world, the counting of photons implies an exactness that their probabilistic description cannot accept.

In the entangled-photon approach, a laser pump directs a stream of photons at a nonlinear crystal (**Figure 4**, **Reference 2**). The incoming photons stimulate the crystal, which then generates and ejects twin photons in opposite directions but having the same quantum states. The approach also involves some optical filtering and special mirror paths. The

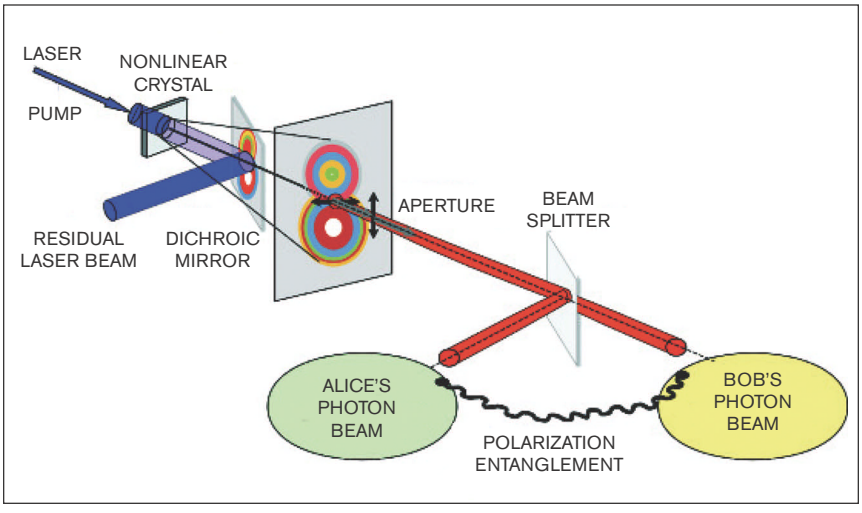


Figure 4 To generate a single photon with known quantum states, a laser's output stimulates a nonlinear crystal, which, in turn, generates twin photons with the same quantum states.

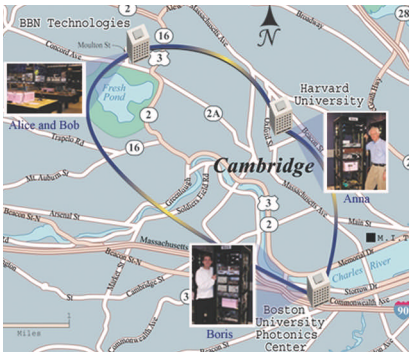


Figure 3 The QC system has two sites in Cambridge, MA—BBN (home to users "Alice" and "Bob") and Harvard University ("Anna")—and a site in Boston at Boston University ("Boris").

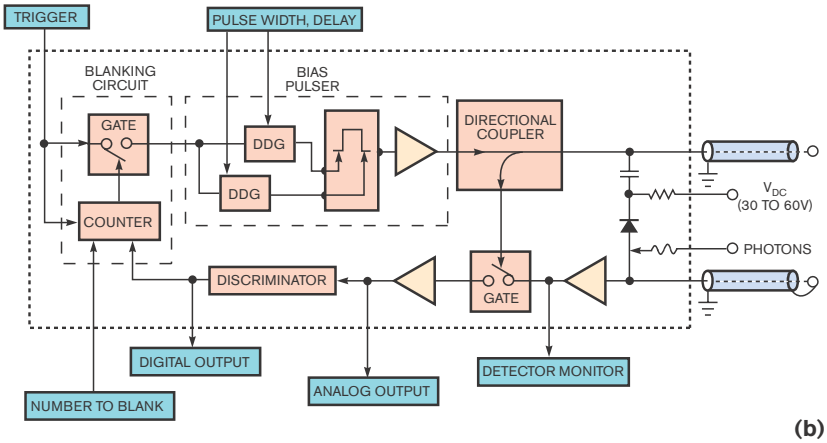
virtue of this system, which BBN also uses, is that, by observing one of the photons, you learn what you need to know about its twin. BBN's Elliott punches the point home with a comment that is familiar to quantum-physics researchers but not to conventional RF and telecom engineers. "You want to be pretty careful when you look at something; it is a conclusive action," he says.

SOURCING IS EASIER

Generating single photons may seem complicated, but it's the lesser of the complementary challenges. "Single-photon detectors are the real nightmares," notes Elliott, and they are currently the limiting factors in system implementation. The well-established silicon-based detector is adequate for visible photon wavelengths of the free-space link, even though you must cool them to −40°C to reduce random noise.

For fiber-based QC links, the BBN system uses an InGaAs/InP (indium-gallium-arsenide/indium-phosphide) photodetector cooled to −50°C. Unfortunately, this detector has low quantum efficiency, converting only 10 to 20% of the photons that hit it into an electrical pulse. To improve performance, Elliott says, the team is building a superconducting detector using niobium nitride, operating at 2 to 4°K. In this type of detector, an incoming photon momentarily kicks the crystal out of its superconducting mode, and the crystal produces a current glitch as a result. These detectors have the potential to run at 10 to 100 GHz, compared with a few megahertz for InGaAs/InP, thus removing one bottle-

(a)



(b)

Figure 5 The custom-built, single-photon detector unit, which IBM Almaden built, has an optical-detector front end (a) and a considerable amount of support electronics (b).

neck to overall system throughput. Cooling the detector material to a few degrees Kelvin is not a problem because, Elliott notes, "It's amazing; you can get a pretty good chiller for $20,000."

A photon-detecting crystal is critical, but it is not the entire front end. The complete single-photon detector is a rack-mount chassis with additional electronics (**Figure 5**); the DARPA Quantum Network built a dozen of these beautiful, handcrafted units at the IBM Almaden Research Center (San Jose, CA), and BBN has six of them. In October, IBM licensed this technology to Princeton Lightwave (www.princetonlightwave.com), to further commercialize QC.

Another pair of key elements of the fiber-based QC link is a set of interferometers—one at the BBN site and one at Harvard—to adjust and match optical-path phases. Their optical lengths must match to less than a fraction of a wavelength, which is a tight requirement. In the current design, a carefully controlled standard power supply applies subtle voltage changes across the lithium-niobate phase modulator that is part of the interferometer, and the piezoelectric effect produces a small but sufficient change in

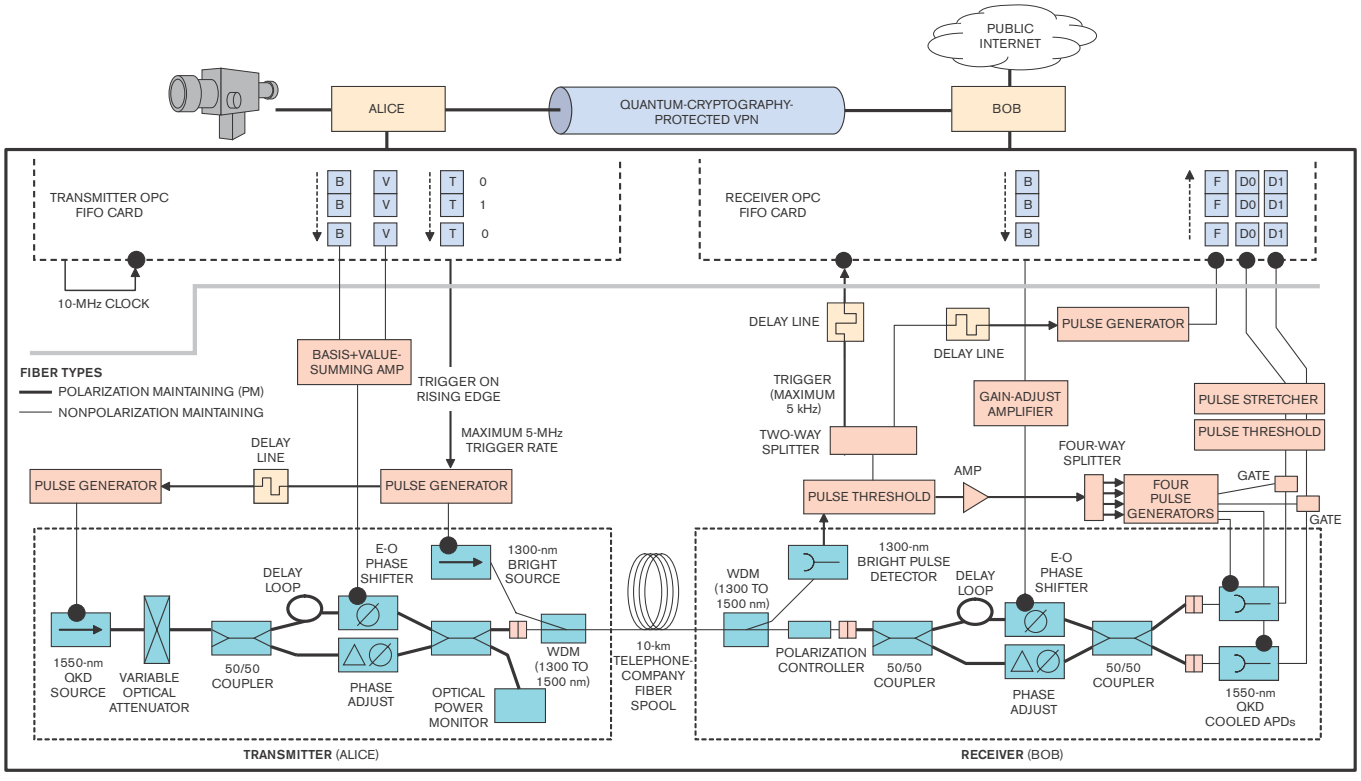


Figure 6 The complete link between Alice and Bob includes all-optical, electronic, and electro-optical elements, including sources, delay lines, phase shifters, couplers, splitters, and optical fibers. The optical fibers include both polarization-maintaining and -non-maintaining fiber.

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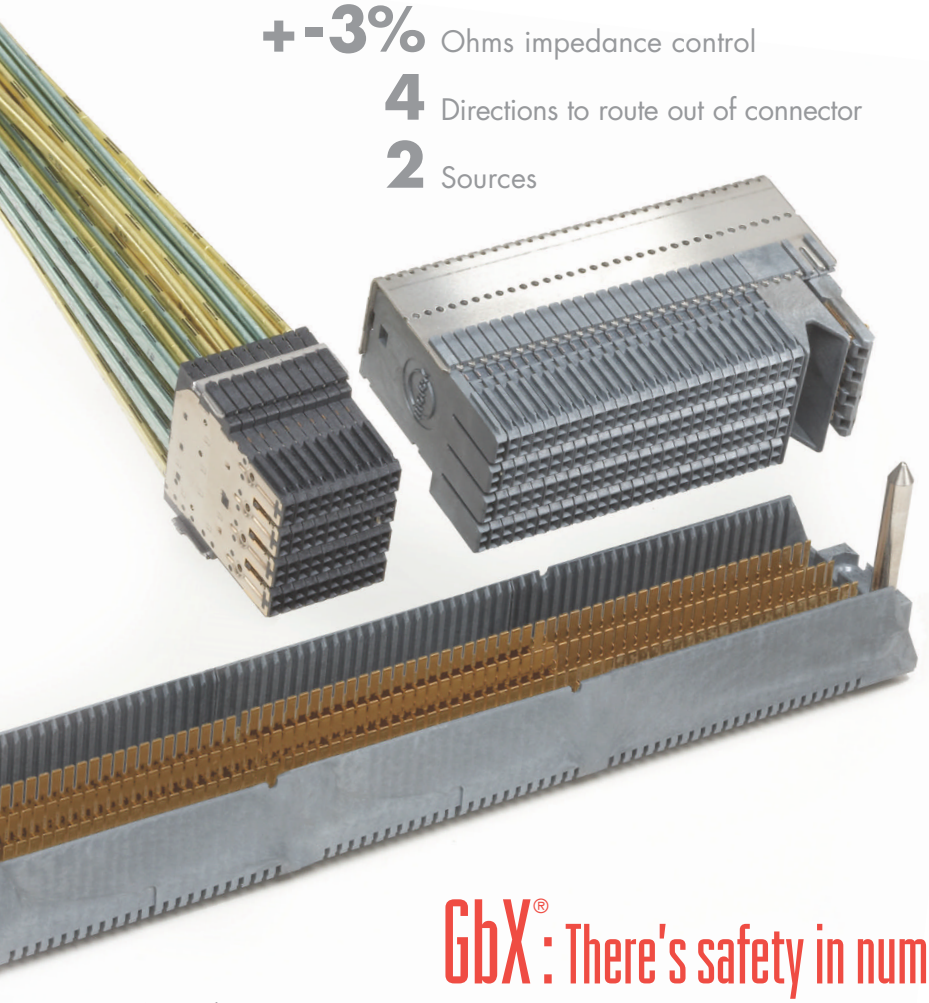

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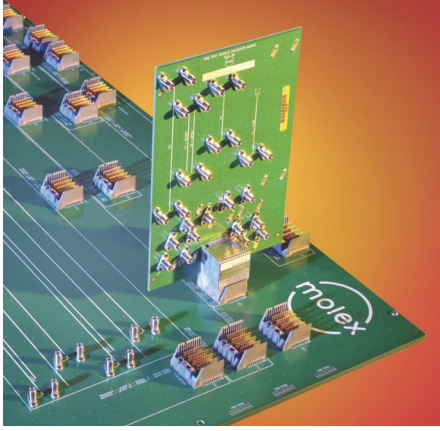

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THINK DIFFERENTLY

For engineers used to thinking of signal power, decibels of attenuation, and meter-based measurement, the quantum world of photons can be a different place. When an optical engineer speaks about attenuating the signal energy or power, the process is not at all like it is for the case of conventional voltage and current signals. The only way to attenuate a photon stream's energy or power is to reduce the *number* of photons, because the energy of a photon is a function only of its wavelength or frequency.

Several quantum states, including polarization and characteristics, define each photon. The basic act of measuring a photon's quantum states may change the values of those parameters, following Werner Heisenberg's uncertainty principle, which states that you cannot simultaneously determine both the positions and the quantum states of particles such as photons. In short, the act of measurement affects the particle you are measuring. In the quantum-physics world, you are not dealing with certainties and absolutes; you are working with probabilities of where the photons are and what parameters they have. This situation contrasts with the well-defined and measurable world that engineers normally associate with their circuits and systems.

the crystal dimension. (A previous version used an independent piezoactuator, but the newer approach is simpler.) An absolutely light-tight box built of 3-in.-thick Styrofoam that you can purchase from Home Depot encloses the entire interferometer; it is the only part of the complete QC link insulated to minimize thermal effects (**Figure 6**).

The single-photon source and corresponding detector are custom-made, as is the interferometer and its box. Most of the remaining extensive setup is standard electronic or optical test, measurement, or processing equipment. As Elliott notes, "The rest is telecom equipment—fast and cheap." He adds, "Most of the equipment is off-the-shelf; you could just about get out your credit card and do it yourself in your basement." This statement is an exaggeration, because the design and implementation contain a tremendous amount of IP (intellectual property), but it does give a sense of how extensively the overall QC system takes advantage of moderate-cost, high-performance electronic- and optical-communication modules and units.

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Despite the overall complexity of the system, it runs on its own with autocalibration, start-up mode, and self-test mode, and it supports continuous data throughput. From a power-up cold start, the entire QC link is ready to use in only about 30 seconds (not including the time for the various PCs used as controllers to boot up their operating systems and drivers), and aligning the interferometers takes up most of this time. The next step, says Elliott, is to put as many of the control functions as possible into FPGAs and reduce the use of PCs, which would make the systems smaller, cheaper, and more hardware-based. EDN

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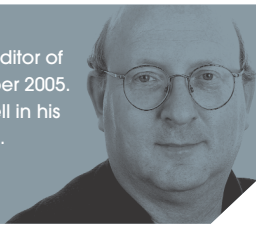

Bill Schweber was Executive Editor of *EDN* until October 2005. We wish him well in his new endeavors.

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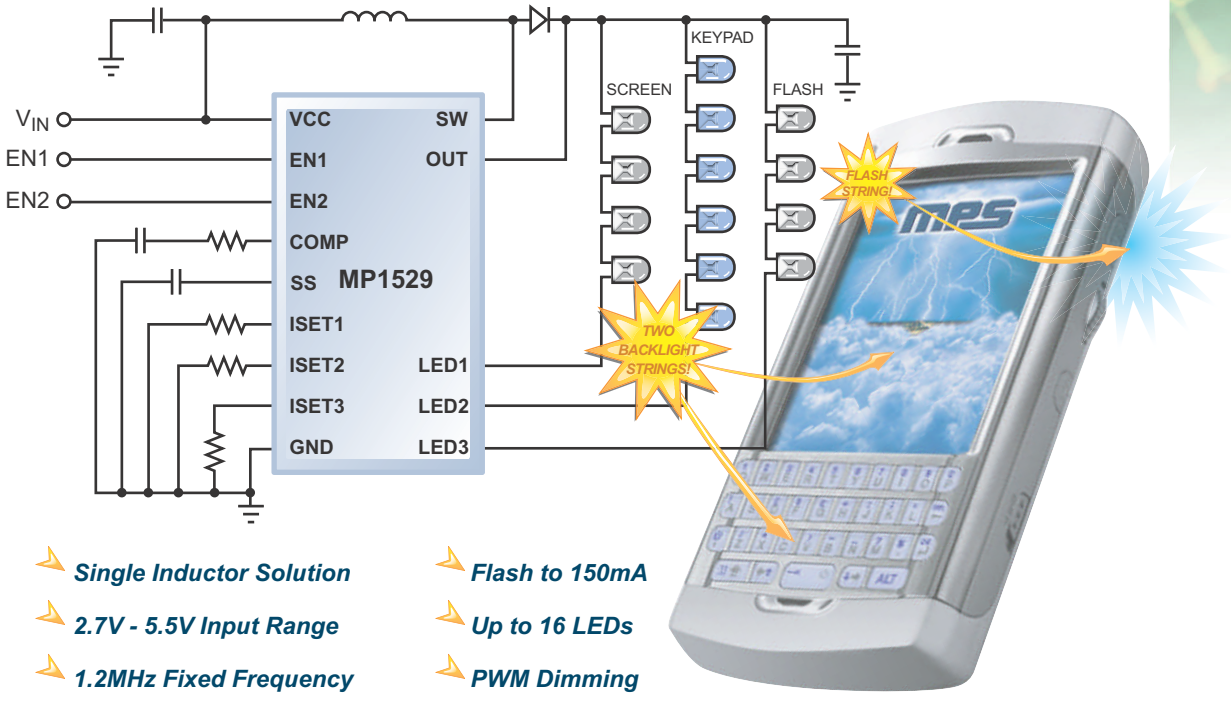

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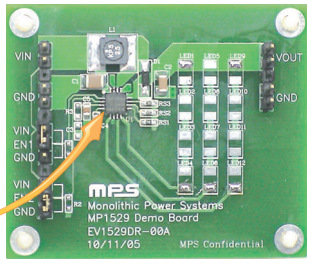
MP3205	2.5 - 6	21	5 / 1	TSOT23-5
MP1518	2.5 - 6	25	6 / 1	QFN8
MP1528	2.7 - 36	38	9 / 1	QFN6
MP1529	2.7 - 5.5	25	16 / 3	QFN16



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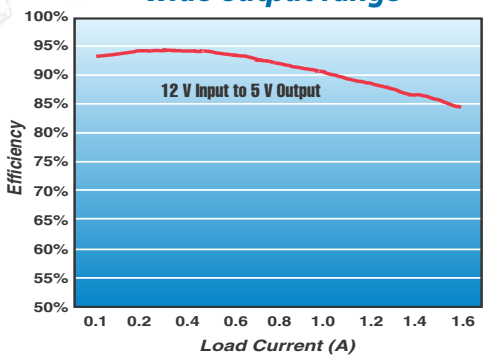
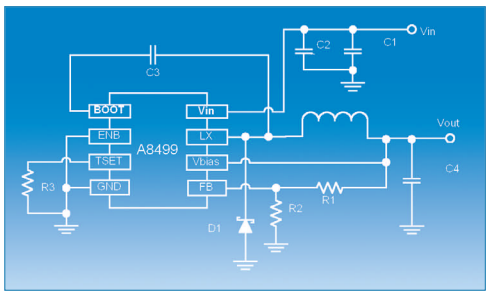
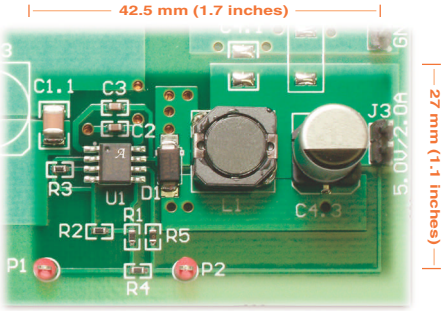




A8499 Application Circuit



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LINEAR TECHNOLOGY

DESIGN NOTES

Monolithic Step-Down Regulator Withstands The Rigors of Automotive Environments and Consumes Only 100µA of Quiescent Current – Design Note 378

Rich Philpott

Introduction

Automobile electronic systems place high demands on today's DC/DC converters. They must be able to precisely regulate an output voltage in the face of wide temperature and input voltage ranges—including load dump transients in excess of 60V and cold crank voltage drops to 4V. The converter must also be able to minimize battery drain in always-on systems by maintaining high efficiency over a broad load current range. Similar demands are made by many 48V nonisolated telecom applications, 40V FireWire peripherals and battery-powered applications with auto plug adaptors. The LT3437's best in class performance meets all of these requirements in a small thermally enhanced 3mm × 3mm DFN package.

Features of the LT3437

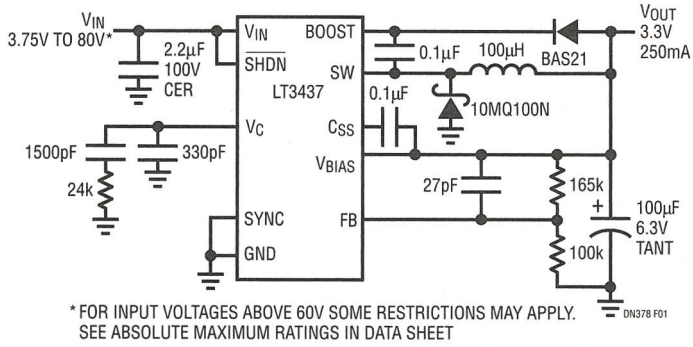
The LT®3437 is a 200kHz fixed frequency, 500mA monolithic buck switching regulator. Its 3.3V to 80V input voltage range makes the LT3437 ideal for harsh automotive environments. Micropower bias current and Burst Mode® operation help to maintain high efficiency over the entire load range and result in a no load quiescent current of only 100µA for the circuit in Figure 1. The LT3437 has an undervoltage lockout and a shutdown pin with an accurate threshold for a <1µA quiescent current shutdown mode.

External synchronization can be implemented by driving the SYNC pin with a logic-level input. The SYNC pin also doubles as Burst Mode defeat for applications where lower output ripple is desired over light load efficiency. A single capacitor provides soft-start capability which limits inrush current and output voltage overshoot during startup and recovery from brown-out situations. The LT3437 is available in either a low profile 3mm × 3mm 10-pin DFN or 16-pin TSSOP package both with an exposed pad leadframe for low thermal resistance.

Brutal Input Transients

Figure 2 shows the LT3437's reaction to the severe input transients that are possible in an automotive environment. Here, the input voltage rises from a nominal 12V to 80V in a 100ms load dump pulse, then drops to 4V in a 150ms cold crank pulse. The 200kHz fixed frequency and current mode topology of the LT3437 allow it to take it all in its stride—response to the input transients are less than 1% of the regulated voltage.

The fuzziness seen on the output voltage is due to the ESR of the output capacitor and the change in inductor current ripple as the input voltage transitions between



* FOR INPUT VOLTAGES ABOVE 60V SOME RESTRICTIONS MAY APPLY. SEE ABSOLUTE MAXIMUM RATINGS IN DATA SHEET

Figure 1. 14V to 3.3V Step-Down Converter with 100µA No Load Quiescent Current

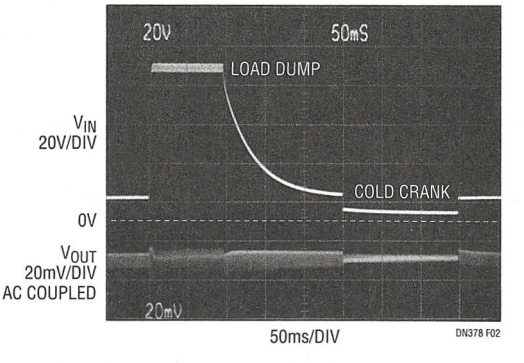


Figure 2. Output Voltage Response to Load Dump and Cold Crank Input Transients

levels. This ripple can be eliminated by changing the output capacitor type from tantalum to ceramic.

Low Quiescent Currents

Many of today's automotive applications are migrating to always-on systems which require low average quiescent current to prolong battery life. Loads are switched off or reduced during low demand periods, then activated for short periods. Quiescent current for the application circuit in Figure 1 is less than 1µA in shutdown mode, and a mere 100µA (Figure 3) for an input voltage of 12V under a no load condition. The LT3437 provides excellent step response from a no-load to load situation as shown in Figure 4. Automatic Burst Mode operation ensures efficiency over the entire load range as seen in Figure 5. Burst Mode operation can be defeated if lower ripple is desired over light load efficiency by pulling the SYNC pin high or driving it with an external clock.

Soft-Start Capability

The rising slope of the output voltage is determined by the output voltage and a single capacitor. Initially, when the output voltage is close to zero, the slope of the output is determined by the soft-start capacitor. As the output voltage increases, the output slope is increased to full bandwidth near the regulated voltage. Since the circuit is always active, inrush current and voltage overshoot are minimized for startup and recovery from overload (brown-out) conditions. Figure 6 illustrates the effect of several soft-start capacitor values.

Conclusion

The LT3437's wide input range, low quiescent current, robust design and small thermally enhanced packages make it an ideal solution for all automotive and wide input voltage, low quiescent current applications.

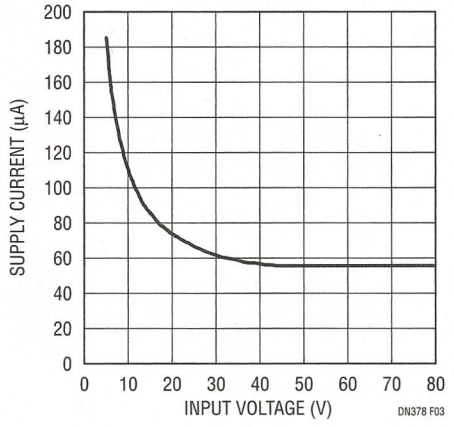


Figure 3. Supply Current vs Input Voltage for Circuit in Figure 1

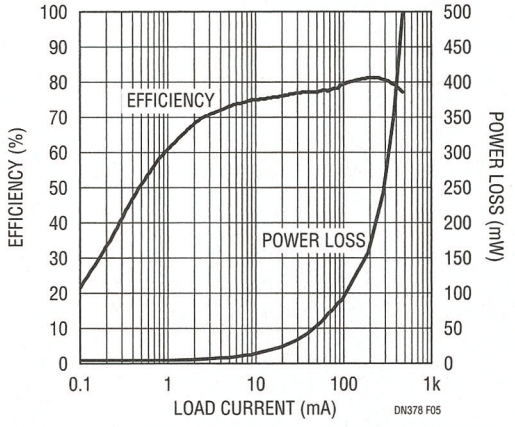


Figure 5. Efficiency and Power Loss vs Load Current for the Circuit in Figure 1

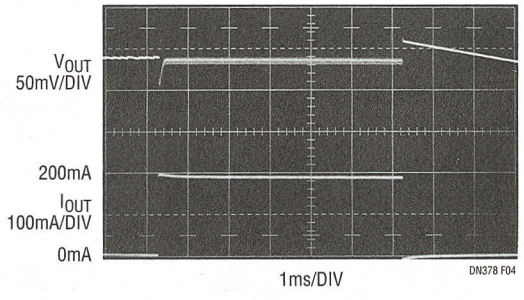


Figure 4. Output Voltage Response for 0mA to 200mA Load Step

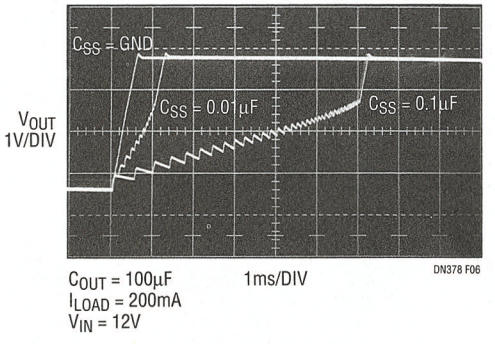


Figure 6. Output Voltage Soft-Start

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BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

GOT GAME?

Living-room consoles grapple for consumers' eyes, wallets

THE HOLIDAYS ARE HERE, SO IT MUST BE TIME FOR ANOTHER ROUND OF GAME-GEAR HYPE. ONLY ONE OF THE NEXT-GENERATION PLATFORMS IS IN PRODUCTION. REGARDLESS OF WHEN THEY EMERGE, THEY ALL PLAN TO EVOLVE THEIR CAPABILITIES BEYOND GAMING WITH AN EYE TOWARD BEING THE HOME'S ENTERTAINMENT CENTERPIECE.

Three years ago, when *EDN* last covered gaming consoles in a Hot Technologies edition, that industry was at a notable inflection point (**Reference 1**). Sony had been shipping its PlayStation 2 in the United States for a little more than a year; the company had launched the PS2 in Japan almost eight months earlier. Microsoft's Xbox was a month old, as was Nintendo's GameCube. Fast-forward three years, and all three consoles are success stories to varying degrees and defined by varying measurement criteria. Look at the Xbox, for example; on the one hand, Microsoft has, according to a recent article, lost $4 billion over the last four years on the console (**Reference 2**). On the other hand, Microsoft reported in January that, by the end of 2004, the Xbox worldwide unit market share was 37%, up from zero two years earlier and against long-established console competitors (**Reference 3**).

The gaming industry had reached another crossroads as this article went to press in late November. Microsoft's Xbox 360, barring a last-minute introduction delay, will, by the time you read this article, have launched in all three primary geographies: the United States on Nov 22, Europe on Dec 2, and Japan on Dec 10, with the first wave of consoles likely sold out (**Figure 1**). Introduction dates for the Xbox 360's primary competitors are unknown; for now, Nintendo will say only that the Revolution

Microsoft hopes that lifelike game environments, along with other factors, will spur consumers to buy in abundance this holiday season and beyond.

AT A GLANCE

- Latest generation living-room game consoles leverage semiconductor and storage innovations, but they must also address socioeconomic dynamics.
- Microsoft hopes to leverage Xbox 360's first-mover advantage to a sustainable leadership position.
- Nintendo's Revolution strives to bring new users into the fold.
- Sony's PlayStation 3 advances both the company's gaming- and movie-format aspirations.

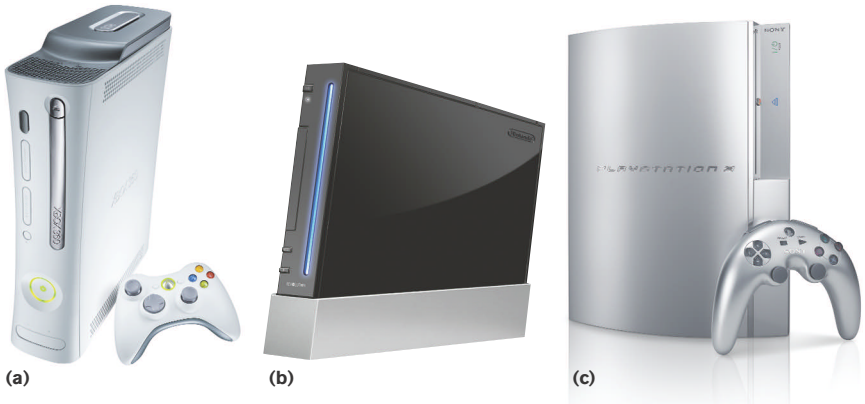


Figure 1 Microsoft's Xbox 360 (a), Nintendo's Revolution (b), and Sony's PlayStation 3 (c) will lead the next-generation console charge into consumers' living rooms.

unveiling won't be until some time after March 2006. However, the company recently asked game-industry insiders to mark their calendars for a May 9, 2006, press briefing—the first day of the E3 conference (Electronic Entertainment Expo, www.e3expo.com). As for the PlayStation 3, a recently published interview with Howard Stringer, Sony's chief executive officer and chairman, hints at a spring-2006 rollout in Japan, with US consumers not getting their hands on the console until the end of next year (**Reference 4**). This year also marked the unveiling of several significant next-generation handheld gaming consoles (see **sidebar** "Next time, portables get their turn").

With every passing generation, the success-or-failure stakes get dicier in the $25 billion gaming business for both hardware manufacturers and content developers (**Reference 5**). Echoing Microsoft's monetary morass, the Playstation 3's development costs reportedly heavily influenced Sony's 46% drop in corporate profits in the second fiscal quarter of this year, compared with that same period a year earlier (**Reference 6**). Mark Thomas, the senior ISV (independent-software-vendor) manager for ATI Technologies, succinctly pointed out in his presentation at October's SID (Society for Information Display) ADEAC (Americas Display Engineering and Applications Conference) that game-development costs are seeing a fivefold increase per generation. (Given the new consoles' significant hardware incompatibilities, those costs are on track to meet or exceed that pace in the games' next iterations.) Meanwhile, only one in 10 games ever turns a profit. And Reggie Fils-Aime, executive vice president of sales and marketing for Nintendo, shared equally disturbing statistics about retrenching trends in the core gaming market during an early-November briefing on the company's DS portable console's WiFi service. (See these statistics at the Web version of this article at www.edn.com/051216df2.)

With all of this gloomy news, why would any sane company seek its fortunes in the gaming business? Because the one title that *is* profitable can potentially far more than make up for the nine that incur losses. In the fourth quarter of 2004, the one quarter that Microsoft's Home and Entertainment division turned a profit, the group's fiscal triumph was the direct result of the mid-November 2004 unveiling of the franchise title *Halo 2*, which earned $125 million in its first *24 hours* on the market and had, by press time, sold more than 8 million copies at roughly $50 a pop (**Reference 7**). One tempting title is often sufficient motivation for a consumer to take the console-purchase plunge. Granted, the hardware manufacturer may sell that console at a loss. But, once the consumer's on the hook, every subsequent game sale is a highly profitable enterprise, either directly—if the console manufacturer also sells the game—or

TABLE 1 KEY FEATURES OF NEXT-GENERATION LIVING-ROOM CONSOLES

	Microsoft Xbox 360	Nintendo Revolution	Sony PlayStation 3
CPU	3.2-GHz Xenon	Broadway PowerPC	3.2-GHz Cell
GPU	500-MHz ATI R500 Xenos and 10-Mbyte frame-buffer DRAM from NEC	Custom ATI design	550-MHz RSX, co-developed by Nvidia and Sony
Memory	512-Mbyte, 700-MHz GDDR3 DRAM	Unknown	256-Mbyte XDR RDRAM and 256-Mbyte, 700-MHz GDDR3 VDRAM
Networking	Bundled CAT5 Ethernet, 802.11a, b, and g as an accessory	802.11b	CAT5 Ethernet (one in, two out), 802.11b/g
I/O	Three USB 2.0, proprietary 2.4-GHz wireless	Two USB 2.0	Six USB 2.0, Bluetooth
Video	Composite and component come standard (component on the high-end-console version). S-Video and VGA cables are accessories.	Unknown	Two HDMI, component, composite
Audio	Dolby 5.1	At least Dolby 5.1	Dolby 5.1, DTS
Storage	Optional removable 20-Gbyte hard-disk drive, two media slots	SD card, 512-Mbyte flash memory	Hard-disk drive, memory stick, SD card, CompactFlash card
DVD media format	Dual-layer DVD	DVD	Blu-ray

through licensing revenue—if the game comes from a partner company. Microsoft forecasts that it will sell 2.7 million to 3 million Xbox 360s in the first three months the console is on the market and 10 million by the end of 2006. Over that initial three-month time frame, Microsoft believes it will earn approximately $1.5 billion in revenue from the sales of not only consoles, but also games, peripherals, and online-gaming subscriptions (**Reference 8**).

Short-term success is exciting, but pragmatic long-term vision is equally important. If Nintendo's data indicating atrophy of the core gaming segment is true, then future growth will need to come from expanding beyond that core by attracting new gamers into the fold, by broadening the console function beyond gaming, or both. From a high-level perspective, the three first-tier next-generation living-room consoles might seem to be "kissing cousins"; Microsoft and Sony based their systems on the same IBM-developed PowerPC core, as Nintendo likely will (**Table 1**). But peer closer, and you'll see significant differences emerge, reflecting each company's unique view of what's necessary for success in this next round of the console wars. There is, however, one other notable similarity: The words "living room" are key parts of each company's strategy. The company whose console becomes the entertainment nexus for the home has control and influence over and, therefore, obtains direct and indirect revenue from, all content flowing into and out of that home.

XBOX 360

By basing the original Xbox on the PC architecture, Microsoft greatly simplified the game-development effort for partners already comfortable with PC-based software projects. However, a PC-derived console also has its fair share of downsides, not the least of which is the relative ease with which the open-PC architecture enables hackers' circumvention of copy protection and other DRM (digital-rights-management) restrictions. Therefore, Microsoft has embraced a PowerPC-based design in the follow-on Xbox 360, and the company has also moved from an Nvidia- to an ATI-developed GPU (graphics-processing-unit) subsystem.

Last time around, partner semiconductor suppliers such as Intel and Nvidia supplied the Xbox silicon building blocks. This time, Microsoft ultimately owns both the design and the manufacturing silicon; it licensed the IP (intellectual property) from other companies. Although the hardware differs in the modern-day Xbox 360 era, Microsoft still hopes to provide some degree of backward-compatibility. Scott Henson, director of the Xbox Advanced Technology Group, indicated in early November that Microsoft is "committed to ensuring compatibility with as many Xbox titles as possible," beginning with those at the top of the popularity list. *Halo 2*, he suggested, is at the pinnacle, and, based on his experience playing it on Xbox 360 hardware a few days earlier, "it runs really well." (Subsequently, Microsoft published a list of more than 200 Xbox titles that consumers can play, using software emulation, on the Xbox 360 at its launch. The goal is that Xbox 360 will support *all* Xbox games.)

IBM developed a die-size- and cost-optimized PPE (PowerPC processing element) processing core for the Xbox 360. Notably, in contrast with a PowerPC core in, for example, an Apple computer, it dispenses with out-of-order execution capability (**Reference 9**). The Xenon CPU in the Xbox 360 contains three PPE cores, each able to simultaneously process two instruction threads and each containing a 32-kbyte, two-way-instruction, Level 1 cache and a 32-kbyte, four-way-data L1 cache, and it also touts the VMX-128 vector-floating-point unit. Each PPE core runs at 3.2 GHz, and they share a common 1-Mbyte L2 cache, which the ATI-developed, GPU-inclusive north-bridge chip can directly access. The cache thereby provides a bridge between the CPU and the remainder of the system. Xenon communicates over a 5.4-Gbps-per-pin front-side bus that can simultaneously read and write at 10.8-Gbyte/sec peak transfer speeds. What will applications do with all that processing power? They will be able to accommodate immersive audio, for one thing; Xbox 360, on the CPU, does the audio processing that a dedicated DSP handled on the first-generation Xbox, and at least one title, *Project Gotham Racing 3*, dedicates an entire CPU core, or two threads' worth of resources, to just audio-related tasks.

NEXT TIME, PORTABLES GET THEIR TURN

Living-room consoles aren't the only commodities that have exciting, controversial, and contending current and future developments. Nintendo's Game Boy Advance SP, Game Boy Micro, and DS portables are squaring off against Sony's PlayStation Portable. Second-tier handheld consoles, such as Tiger Telematics' Gizmodo, are also competing for users' eyes and wallets, as are alternative platforms and potential platforms, such as PDAs, premium-featured cell phones, and enhanced portable multimedia players. Stay tuned for *EDN*'s Jan 19, 2006, issue, in which we'll "go mobile" and explore this segment of the game market in more detail.

ATI delivered its 500-MHz Xenos GPU to Microsoft 16 months after signing the development contract (a time frame only one month shorter than the one IBM accomplished with Xenon). The dual-die Xenos design has impressive peak-performance specifications, including 24 billion shader instructions/sec, a 4 billion-pixel/sec fill rate, and a 500 million-triangle/sec geometry-processing rate. Xenos comprises 250 million transistors in the main, TSMC-fabricated and logic-centric die and 80 million transistors in the daughter die that implements the 10-Mbyte, NEC DRAM-based frame buffer. Today's PC-targeted GPUs contain dual sets of shader processors, one handling vertex operations and the other handling pixel—that is, "fragment"—tasks. Xenos, conversely, includes 48 unified shaders that tackle either vertex or fragment processing, along with other functions, such as physics and video processing using the console's enhanced variant of the DirectX v9 API (**Reference 10**). ATI Vice President of Engineering Robert Feldstein admits that the company's embrace of a unified-shader approach

wasn't risk-free; specifically, there was concern that the task-switching delay between vertex and fragment algorithms might hinder the chip, performancewise. Feldstein happily reports that real-life performance results are even better than simulations suggested and that the company's future-generation PC-graphics chips, along with, he predicts, those of primary competitor Nvidia, will also migrate to a unified-shader approach.

With the first-generation Xbox, a few games ended up supporting a greater-than-480-line display resolution, but CPU-plus-GPU horsepower was generally insufficient to throw additional pixels on the screen at an adequate frame rate and maintain a rich and engaging gaming experience in all other necessary respects. Xbox 360 games, in contrast, must support wide-screen, 720-line progressive resolutions by default. (Note, however, that preliminary screenshot evidence suggests that at least one game, *Project Gotham Racing 3*, is a native *600-line*-resolution title.) The games' developers handle 4-to-3 aspect-ratio displays using either letterboxing or pan-and-scan cropping. The Xenos GPU takes care of downscaling to 480-line or upscaling to 1080-line interlaced resolutions. It also supports progressive-scan DVD playback, a capability that the first-generation Xbox lacked, and also upscales and antialiases Xbox titles, such as *Halo* and *Halo 2*. Microsoft has decided, at least in the near term, to omit a blue-laser-based optical drive. Instead, Xbox 360 contains a mainstream, dual-layer, 12×, red-laser DVD drive (**Reference 11**). Users can currently achieve a high-definition video display on Xbox 360 in two ways: by downloading WMV (Windows Media Video)-encoded films from partners such as CinemaNow and Movielink to the console's hard-disk drive or by using the console's built-in Windows Media Extender capabilities to play video off a Windows XP Media Center Edition-based PC's hard-disk drive. (Additional ways to achieve this high-definition display may come in the future, such as playing a red-laser DVD encoded with Microsoft's WMV or derivative VC-1 formats.) Whereas Microsoft restricted the Windows Media Extender add-on for the Xbox, along with stand-alone Extenders now available in the market, to standard-definition video with two-channel audio, Xbox 360's capabilities remove both constraints. Xbox 360 owners can also access audio and still-image content—although not currently video content—stored on a Windows XP- and Windows Media Connect-based PC or on another UpnP (Universal Plug 'n' Play)-supporting network device.

Xbox 360 will at least initially come in two product variants in the United States. The $299 "Core" version doesn't include the 20-Gbyte, removable hard-disk drive that is necessary for playing first-generation Xbox titles, and it supplies a conventional wired controller. The $399 variant comes with the hard-disk drive, along with a remote control, headset, and additional audio/video and network cabling. All of these features, along with an 802.11a/b/g wireless network adapter, a camera, and other accessories, are also available separately. This version also switches to a wireless controller based on a proprietary 2.4-GHz protocol. Xbox 360 purchasers will automatically be eligible for free Xbox Live Silver accounts, which allow them to maintain Friends lists and send and receive text and audio messages from other Live members, purchase additional game features and online arcade games, and automatically obtain game- and console-firmware updates. Update capability is critical for Microsoft and its content partners, allowing them to stay one step ahead of

TABLE 2 ESTIMATES OF INITIAL AND THREE-YEAR-LATER XBOX 360 BILL-OF-MATERIALS COSTS

Xbox 360	Component	Estimated cost at launch	Estimated cost after three years
CPU	IBM PPC	$100	$35
GPU	ATI GPU	$100	$30
Optical media	DVD-ROM	$25	$10
Memory	512-Mbyte GDDR3	$50	$25
Hard-disk drive	Detachable 20-Gbyte hard-disk drive	$25	$15
USB	Three ports	$5	$3
Ethernet	Ethernet	$5	$4
Wireless controller transceiver	Proprietary 2.4 GHz	$5	$3
Controllers	As many as four wireless	NA	NA
Other	Analog IC, ASICs, I/O	$25	$20
Total		$340	$145

TABLE 3 ESTIMATES OF INITIAL AND THREE-YEAR-LATER PLAYSTATION 3 BILL-OF-MATERIALS COSTS

PlayStation 3	Component	Estimated cost at launch	Estimated cost after three years
CPU	IBM Cell	$160	$50
GPU	550-MHz Nvidia RSX	$100	$30
Optical media	Blu-ray	$100	$30
Memory	256-Mbyte XDR/256-Mbyte GDDR3	$60	$30
Hard-disk drive	Detachable 2.5-in. hard-disk drive	NA	NA
USB	Six ports	$5	$3
Ethernet	Gigabit Ethernet	$5	$4
WiFi	802.11b/g	$5	$3
Bluetooth	Bluetooth 2.0	$10	$5
Other	Analog IC, ASICs, I/O	$50	$40
Total		$495	$195

DRM hackers (**Reference 12**). Full-blown Xbox Live Gold account holders can engage in online multiplayer gaming, among other service enhancements.

REVOLUTION

A lot of detailed information on Microsoft's next-generation console is public, and a large chunk of that information has been public since mid-May's E3 (Electronic Entertainment Expo) conference. This is not the case with Nintendo, which, trivia buffs might be interested to know, released its groundbreaking NES console in the United States 20 years and six months ago; *Mario* turned 20 years old in September. The company's next-generation console's official name hasn't even been unveiled yet; Revolution is just a project-name placeholder. Revolution will employ an IBM-developed PowerPC CPU. However, it's still unknown how many cores and what else that CPU will contain; how many threads each core will process; and whether the core will be the PPE that Microsoft and Sony are using, an Apple- or Xilinx-reminiscent core, or something completely new. And Revolution will, like the Xbox 360, contain ATI Technologies-developed graphics. Again, though, aside from revealing that Revolution will not support high-resolution video-output capability, Nintendo has released no specifications except, presumably, to software developers under NDAs (nondisclosure agreements).

What Nintendo has revealed, however, in conjunction with corporate executives' big-picture comments, strongly suggests that the company is taking a clean-slate approach to the console- and corresponding content-development processes. At E3, Nintendo gave the public, among other things, a first glimpse into the console's case design, which will be available in multiple color options, and indicated that it will be able to both play Revolution-native, DVD-based games and legacy GameCube titles on the proprietary small-diameter optical disc. At the follow-on Tokyo Game Show in mid-September, Nintendo's President Satoru Iwata unveiled the console's controller (**Figure 2**). Judging from the promotional video clip that Nintendo released at the time, the console will be able, most likely by using RF-based triangulation, to determine and respond to the "nunchaku-style" controller's position in 3-D space, and its direction and speed of motion, in addition to the user's manipulation of controller buttons (**Reference 13**).

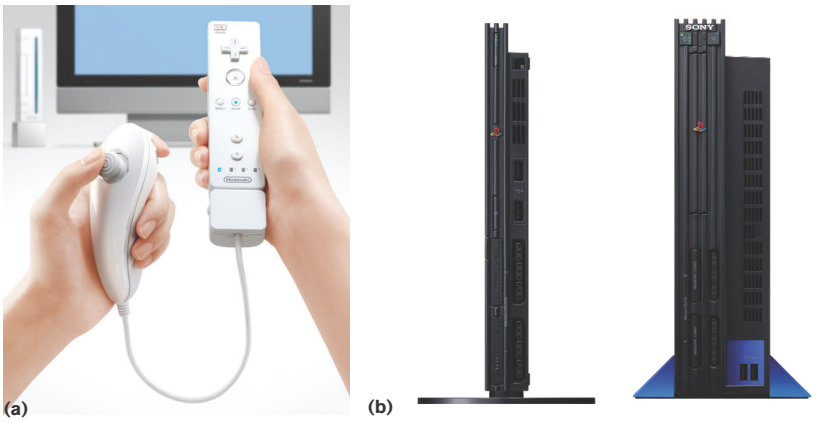


Figure 2 Nintendo's aspirations for future living-room success hinge on innovations such as the Revolution's controller (a), whereas Sony for now will have to hope that a slimmer–and, potentially, cheaper–PS2 console will be enough incentive to extend the lifetime of its current, four-year-old franchise, until the PlayStation 3 is ready to ramp (b).

The video clip showed Revolution players, among other things, chopping food and stirring it in a wok, fishing, playing the drums, holding a flashlight, swatting flies, and conducting a symphony orchestra. These are notably nontraditional console applications, and many of the players are equally nontraditional: the very young, the very old, and mixtures of the two, suggesting the family and communal collaboration opportunities that Revolution will encourage. Even in the more traditional gaming genres in the video clip, such as hitting a ball with a racquet or a bat, shooting a pistol, sword-fighting, and making *Mario* jump, Nintendo portrayed the Revolution's controller as enabling players to implement these actions in innovative ways. And, Nintendo will also sell an accessory that provides a more conventional control layout when a user slips a controller into it. This accessory will satisfy both the desires of traditional developers and players and the need for backward compatibility with GameCube.

None of these scenarios is terribly surprising; Nintendo has a long history of designing hardware and software that consumers can pick up and quickly and intuitively begin using with little to no perusal of tedious and time-consuming instructions. Nintendo argues that Microsoft and Sony, with their latest offerings, instead focus on technology for technology's sake. Neither the Revolution controller's similarity to a TV remote control nor the console's placeholder name is coincidental. Quotes from Iwata throughout this year echo the statistics Nintendo shared with the press in early November, and they further flesh out the company's direction with Revolution. These quotes include:

"If we cannot expand the market, all we can do is wait for the industry to slowly die," "it is our responsibility to make games for all skill levels ... including people who are not playing games now," "technology alone can't advance video games ... which is why we plan to take Revolution in a dramatic new direction," and "Revolution ... does not follow the conventional path of new game systems."

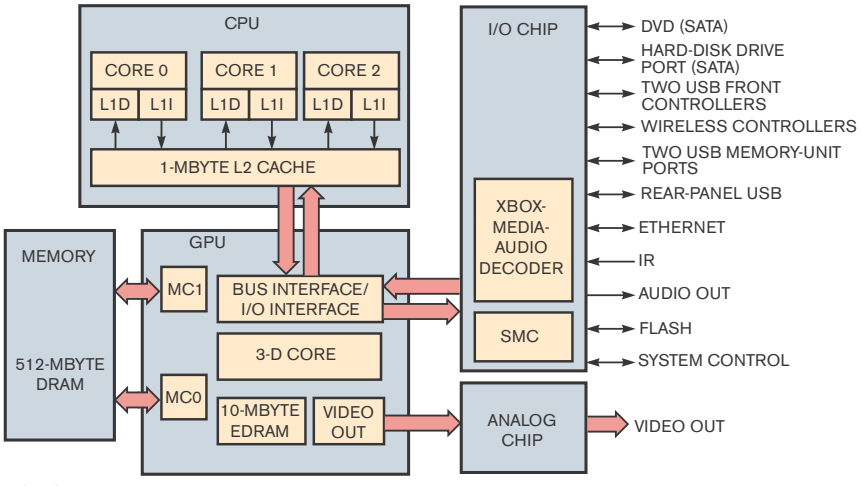
How much will Revolution cost? Again, specifics aren't public, but Fils-Aime in early November said, "Certainly, from the standpoint of being a single-minded gaming device, it will absolutely be much more affordable than any of the other competing systems."

PLAYSTATION 3

The discrepancies between Microsoft's Xbox 360 and Sony's PS3 (PlayStation 3), whose release schedule and price aren't yet public, begin with their CPUs (**Figure 3**). The Cell CPU swaps out two of the three Xenon PPEs, along with half of the L2 cache, for eight SPEs (synergistic processor elements). Only seven of the eight SPEs in Cell are developer-accessible in PlayStation 3; at E3, Sony

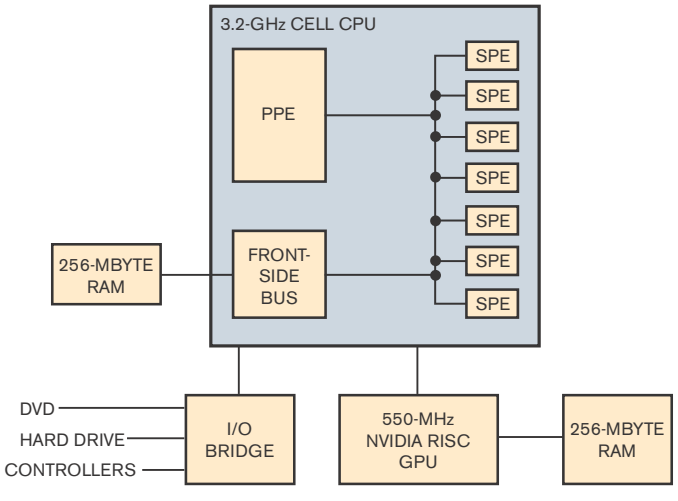
indicated that it reserved the eighth SPE for "redundancy," suggesting that the lack of a full complement of SPEs was a yield-boosting and cost-saving maneuver. More recent rumors, however, suggest that the eighth SPE is fully operational, but the PS3 reserves it for DRM or other operating-system-controlled functions. The Cell SPE performs single-precision SIMD (single-instruction-multiple-data) computation, and each SPE partners with 256 kbytes' worth of dedicated single-port instruction SRAM.

Sony, in competitively positioning Cell against Microsoft's Xenon, vigorously touts its processor's greater-than-200-Gflops' worth of single-precision peak computational capability (with all eight SPEs enabled) and at 3.2 GHz. Microsoft counters with Xenon's more "balanced"



NOTES:
L1D=LEVEL 1 DATA CACHE.
L1I=LEVEL 1 INSTRUCTION CACHE.

(a)



NOTES:
PPE=POWERPC PROCESSING ELEMENT.
SPE=SYNERGISTIC PROCESSOR ELEMENT.

(b)

Figure 3 Peer closely, and you'll find several significant architecture discrepancies between the Xbox 360 (a) and PlayStation 3 (b), reflecting the companies' philosophical differences on partitioning.

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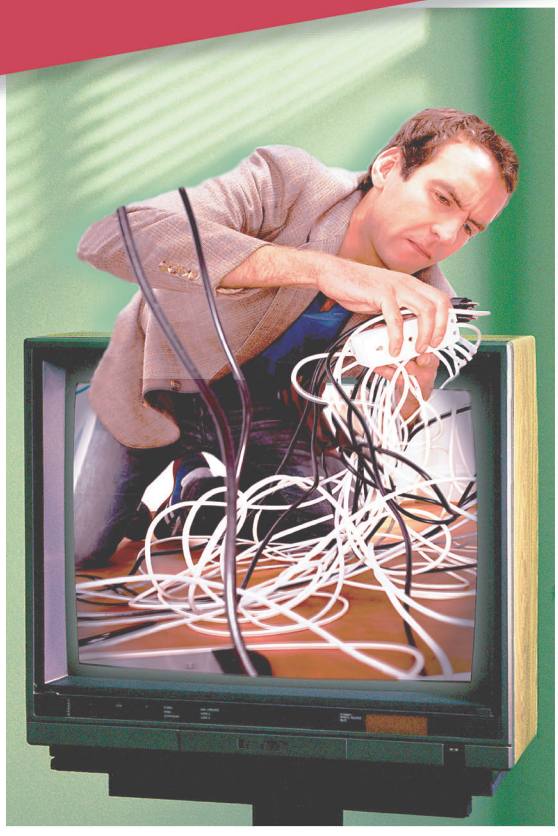

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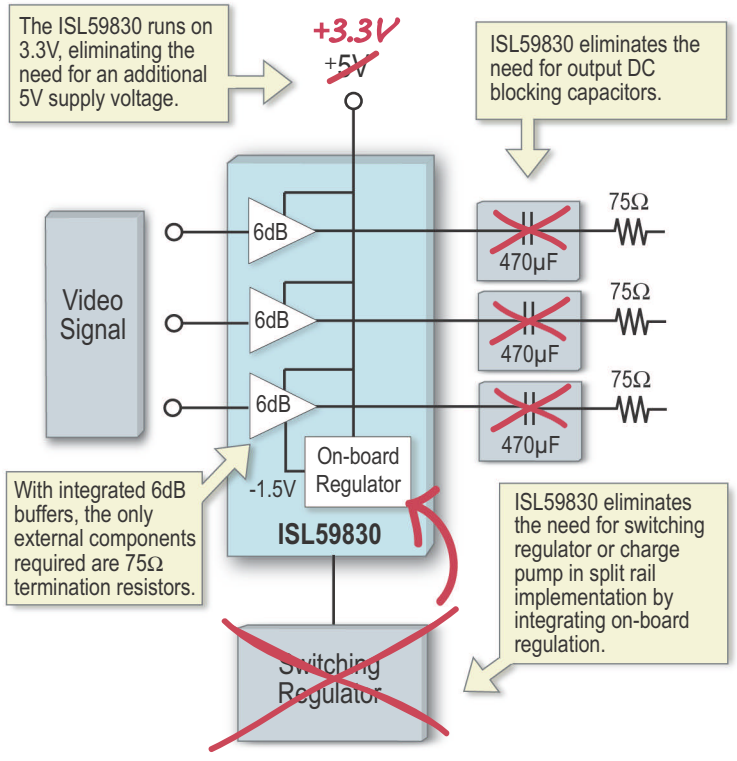
ISL59830 Functional Block Diagram



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multicore approach, 9 billion-dot-product-operations/sec capability, and "greater than one teraflop of system floating-point performance." The Xbox 360's floating-point specification sums both the CPU's and the GPU's capabilities (**Reference 14**). The Cell and Xenon have 235 million and 165 million transistors and 235- and 168-mm^2 die sizes, respectively, both at 90-nm process geometries. These specifications are instructive for folks who want to make cost and yield forecasts. ATI Technologies is also quick to point out that Microsoft is using a console-optimized GPU, whereas rumors have it that the PS3's RSX is nothing more than a 90-nm shrink of Nvidia's PC-tailored GeForce 7800 GTX, which Nvidia slightly tweaked to mate up to the Cell's BIC (bus-interface controller) rather than a PC's PCI Express bus.

What, if anything, do the specification, feature, and partitioning differences between the two consoles translate to in actual game playing? It's impossible to say with any degree of certainty, because Sony has yet to publicly demonstrate actual hardware running actual game code. Sony has to date showcased only prerendered game sequences and video clips that the company claims show the console spitting out pixels, along with an E3 video clip purportedly demonstrating that a single Cell processor can simultaneously decode 48 standard-definition MPEG-2 streams, downscale each of them by a factor of nine, and display them tiled within a 1920×1080-pixel HDTV window.

Microsoft's Corporate Vice President J Allard gleefully points out that all the PS3 consoles and pictures of consoles that Sony has shown the public so far lack ventilation holes, suggesting that they're mechanical mockups with no functional chips or other hardware inside. Conversely, Microsoft invited the public to testdrive early Xbox 360 game code at the mid-May E3, running on G5 Power Mac console-emulation systems. Microsoft began shipping Xbox 360 hardware to developers at the end of June; demonstration systems started arriving at US retailers, such as EBGames, GameStop, and Wal-Mart, in mid-October; and Microsoft opened the Xbox Lounge demo facility in the Omote Sando district of Tokyo at the same time. Perhaps Sony will finally show functional PS3s at next month's Consumer Electronics Show in Las Vegas.

At E3, Sony mocked Microsoft's reluctance to definitively assure consumers of the Xbox 360's full compatibility with first-generation Xbox titles. However, more recent data suggests that Sony may be in the same boat; the latest slim variant of the PlayStation 2 doesn't play all PlayStation 2 titles, due to cost-slimming internal-circuitry changes that Sony made, and Sony officials don't rule out similar limitations in the PlayStation 3. Skeptics also point to a patent Sony received late last year, which describes "A device and method for protection of legitimate software against used software and counterfeit software in recording media ... A specific title code is read, and if this title code has been registered, the main unit shifts to a normal operation. If the code has not been registered, verification software is initiated ... If matching does not occur, the disk is processed as illegitimate software ... Since only titles for which legitimate software has actually been purchased and which have been initially registered in the machine table can be used, resale (so-called used software purchase) after purchase by an end-user becomes practically impossible" (**Reference 15**). In other words, if Sony were to apply this technique to the PlayStation 3, a game would be playable only from the console in which it first resided, thereby squelching not only game piracy, but also the used- and rental-game markets, and

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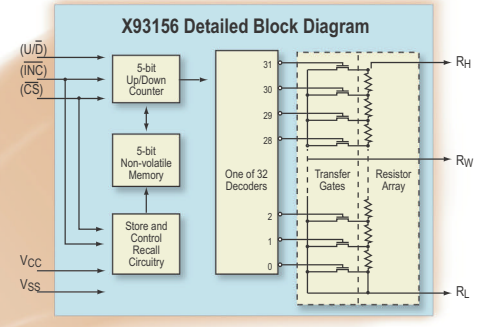

Features

- 3-wire up/down interface
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- Low power CMOS, with V_{CC} of 2.7V to 5.5V, active current of 250µA max, and standby current of 1µA max
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- Available in 8-lead MSOP and TDFN packages
- Pb-free and RoHS compliant packaging available

Key Parameters

Description	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	X93154	2.7	3	3.3	V
	X93155	4.5	5	5.5	V
	X93156	2.7	-	5.5	V
End-to-end Resistence		35	50	65	kΩ
R_H, R_L Terminal Voltages		0	-	V_{CC}	V
Power Rating	R_{TOTAL} = 50 KΩ	-	-	1	Mw
Noise	Ref: 1kHz	-	-120	-	dBV
Wiper Resistance	X93156	-	-	1100	Ω
Wiper Current		-	-	0.6	mA
Resolution		-	3	-	%
Temperature (Industrial)		-40°C	-	+85°C	C

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even game-trading with friends.

Sony intends for PlayStation 3 to be much more than a gaming console. Among other things, it will act as a Trojan horse to get the company's championed blue-laser optical-storage format, Blu-ray, into consumers' homes worldwide. The game-subsidized console will likely be much less expensive than the first generation or few of stand-alone Blu-ray players. But Blu-ray's relative immaturity versus red-laser DVDs will fiscally burden PS3; some estimates place the cost of the Blu-ray drive alone at more than $100 (**Reference 16**). More generally, investment firm Merrill Lynch recently predicted that "PS3 will not only be significantly more costly than Xbox 360 at launch, but will continue to operate at a cost disadvantage for several years" (**Reference 17**). The company's detailed cost analysis reveals the added burden Sony is shouldering versus Microsoft, due to factors such as the Blu-ray drive, larger die CPU, and Rambus DRAM. This burden will still be present three years into both consoles' high-volume production ramps (**tables 2** and **3**). A subsequently published analysis of the Xbox 360 by iSuppli was more pessimistic about Microsoft, estimating that the at-launch bill-of-materials cost of the console's $399 Premium configuration would be $525 (**Reference 18**).

Console profitability for Sony will depend on price, which has yet to be announced, but the higher the price, the lower the potential sales volume of consoles, games, and Blu-ray movies sold and, consequently, the slower the cost-reducing pace due to volume efficiencies, lithography reductions, and the like. Sony hasn't yet announced whether PS3 will come with a hard-disk drive. Like Microsoft, the company may create two SKUs (stock-keeping units) with the hard-disk drive as a separate accessory on the lower priced console. Sony has recently announced that it will not offer a centralized game-server service, such as Xbox Live, but instead, as with PS2, rely on game developers to implement their own online capabilities (**Reference 19**). This move will reduce costs but will also reduce revenue and, potentially, profit. It is a bit surprising, for two reasons: With games such as *EverQuest*, Sony has shown that it has the expertise to create such a service. Second, competitors Microsoft and Nintendo, which plans to offer the Virtual Console for purchasing and storing downloadable versions of legacy console games on Revolution's flash memory, see online services as key to the communal experience, along with the profits, they're attempting to cultivate. Microsoft even rolled an Xbox Live development environment into its Xbox 360 software-development kit so that console users will have a consistent, rich experience on Xbox Live. EDN

You can reach Senior Technical Editor Brian Dipert at 1-916-760-0159, bdipert@edn.com, and www.bdipert.com.

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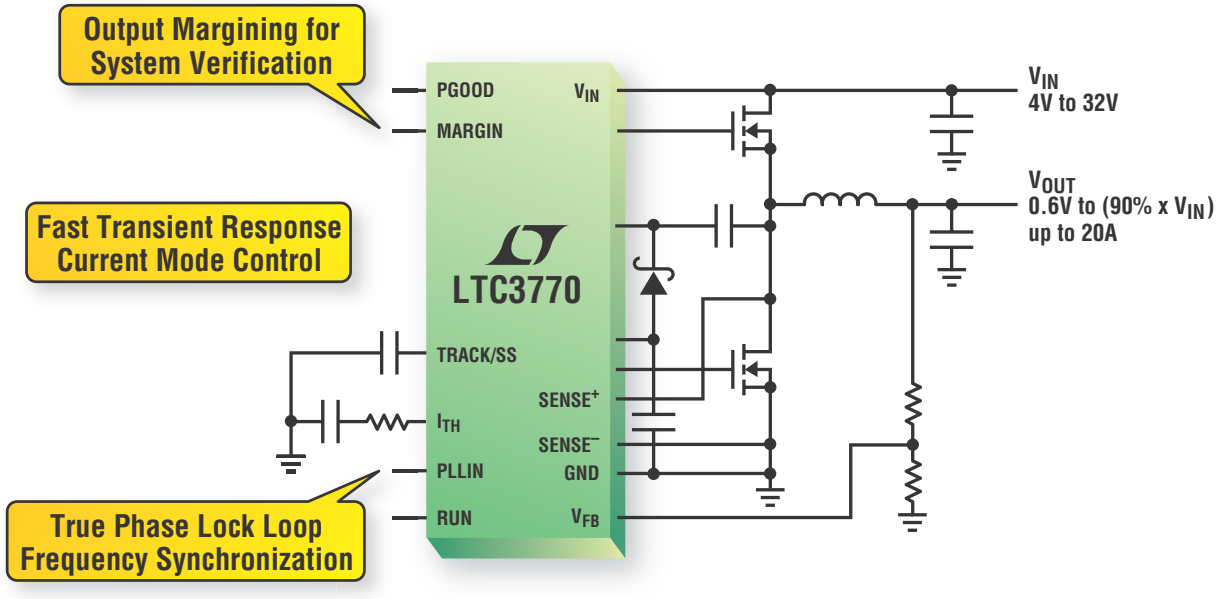

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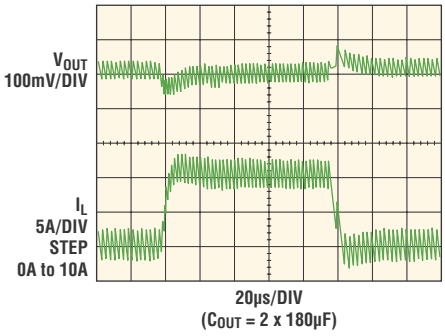

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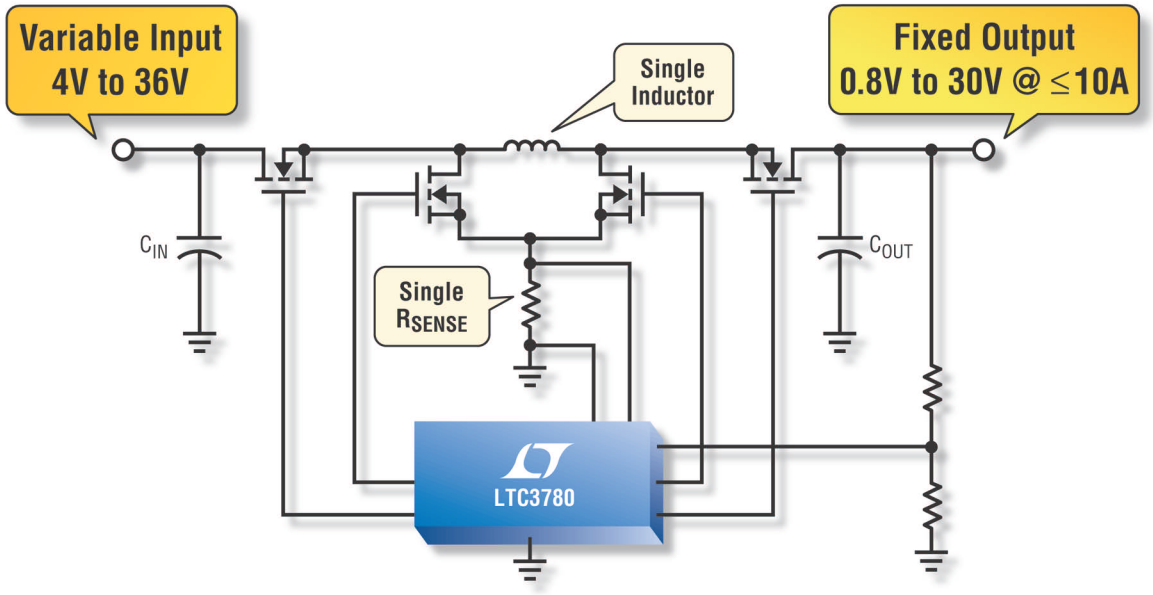

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LTC3780 Efficiency vs SEPIC
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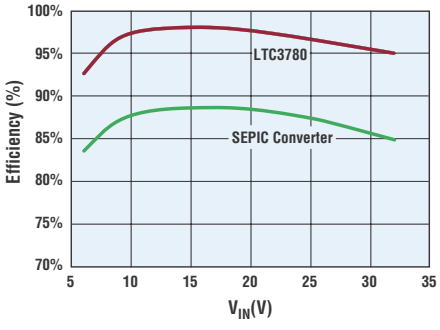

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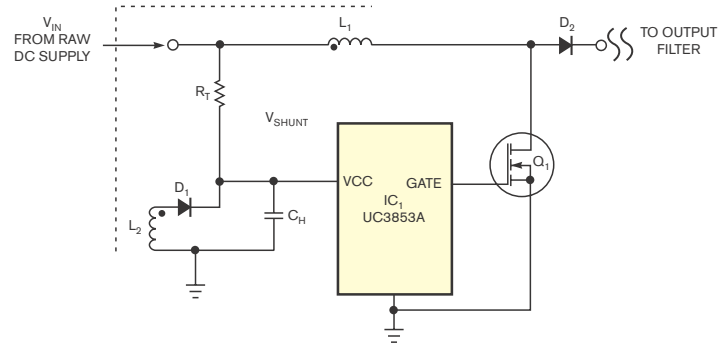
designideas

READERS SOLVE DESIGN PROBLEMS

Shunt regulator speeds power supply's start-up

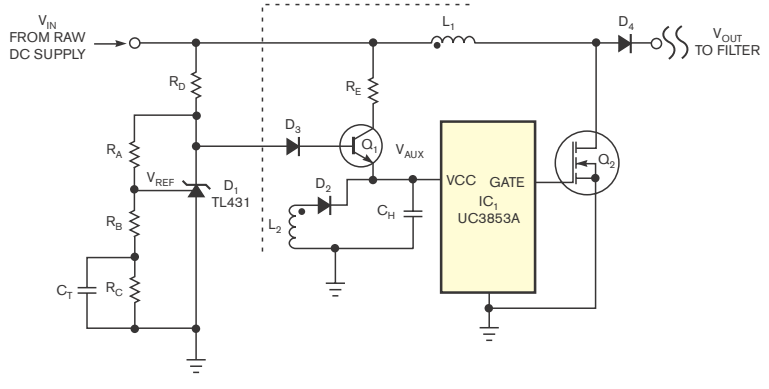
Michael O'Loughlin, Texas Instruments, Nashua, NH

In certain applications, design requirements may call upon a system's switched-mode power supply to more promptly deliver its output than would the garden-variety power supply. **Figure 1** shows such a supply's bootstrap, or start-up, circuit. In a switched-mode power supply's PFC (power-factor-corrected) preregulator, the circuit's PWM (pulse-width modulator), IC_1, draws its normal operating power from auxiliary winding L_1, wound on boost inductor L_2's magnetic core and diode D_1.



NOTE: DASHED LINE SHOWS MAGNETIC COUPLING BETWEEN WINDINGS L_1 AND L_2.

Figure 1 In a conventional switched-mode power supply's bootstrap circuit, trickle-charge resistor R_T and capacitor C_H supply start-up power to the pulse-width modulator and controller, IC_1.



NOTE: DASHED LINE SHOWS MAGNETIC COUPLING BETWEEN WINDINGS L_1 AND L_2.

Figure 2 In this augmented bootstrap circuit, transistor Q_1 delivers a robust initial pulse of current to capacitor C_H, ensuring faster start-up and power delivery.

DIs Inside

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Resistor R_T and capacitor C_H form a trickle-charge circuit that supplies power for bootstrapping IC_1 into normal operation. In conventional designs, R_T comprises a high resistance that delivers just enough current to overcome the standby current and supply a trickle charge to holdup capacitor C_H, which stores enough energy to power the PWM circuit until the power converter begins operation. Under normal circumstances, the circuit's slow start-up response poses no problems.

When faster power-on response becomes important, you can reduce the bootstrap time by reconfiguring the start-up shunt regulator (**Figure 2**). Capacitor C_T; shunt-regulator IC D_1, a TL431; diode D_3; transistor Q_1; and resistors R_A through R_D form the bootstrap circuit. At power application, capacitor C_T holds no charge, and the series-pass regulator that Q_1 and D_1 form determines the voltage at the PWM's power input, V_{AUX}.

At turn-on, the V_{AUX} voltage reaches its peak voltage, V_{AUX_PEAK}, which the ratio of resistors R_A and R_B determines.

Capacitor C_T and resistor R_C conserve energy by setting the bootstrap circuit's turn-off time and voltage. Resistor R_D supplies bias current to D_1, the TL431 shunt-regulator IC, and resistor R_E keeps transistor Q_1 within its safe operating area by limiting its collector current.

To design the circuit, begin by selecting resistors R_A and R_B to establish the peak charging voltage, as the following equation shows:

$$\frac{V_{REF}}{R_B} = \frac{V_{AUX\_PEAK} + V_{D3} + V_{BE} - V_{REF}}{R_A + R_B},$$

where V_{REF} represents the TL431's internal reference voltage. Next, select resistor R_C to reduce the shunt-regulated voltage below the nominal V_{AUX} voltage, $V_{VAUX\_NOMINAL}$, which the auxiliary winding supplies:

$$RC_T = \frac{V_{REF} \times R_A + (V_{REF} - V_{AUX\_NOMINAL})R_B}{V_{AUX\_NOMINAL} - V_{REF} - 1V}.$$

Choose capacitor C_T's value to set the bootstrap time, T_{BOOT}, as follows:

$$C_T = \frac{2 \times T_{BOOT}}{R_C}.$$

As in **Figure 1**, diode D_2 and auxiliary winding L_2 provide normal operating power to IC_1. EDN

Build a USB-based GPIB controller

Boštjan Gla ar, Marko Jankovec, and Marko Topic,
Laboratory of Semiconductor Devices, Ljubljana, Slovenia

Contemporary research laboratories include a variety of instruments that connect using any of several interface methods to a PC for automating procedures and collecting data. Although different communication interfaces exist, the GPIB (general-purpose-interface bus) still enjoys wide popularity. The host PC must include a suitable GPIB controller—an internal interface card or an external device. Newer PC designs are phasing out traditional internal buses, such as PCI, ISA, and EISA, in favor of other standards, so using an external controller offers a more appropriate approach because external I/O ports, such as RS-232 and USB, tend to maintain backward compatibility.

This Design Idea covers the development of a GPIB controller, which turned out to be easier and cheaper than commercially available alternatives. The design uses easy-to-obtain components with a total component cost of approximately $50. For comparison, a commercial controller costs at least 10 times more: $500 to $1000. The USB 2.0-compliant controller, an external device, draws its operating power from the bus and provides plug-and-play operation and high-speed data transfer. In addition, a USB-controller design extends its applications to notebooks and other computers that lack available I/O slots. The controller resides on a double-sided pc board and fits into a 123×30×70-mm enclosure (**Figure 1**). To simplify controller use, the design uses National Instruments' (www.ni.com) LabView graphical programming language to develop the appropriate driver.

The design uses the FT245BM USB-controller IC from Future Technology Devices International Ltd (www.ftdichip.com), which features an 8-bit parallel connection to the host microcontroller and a virtual-communications port to the PC-interface side. The circuit operates at a full speed of 12 Mbps. Targeting use in GPIB applications, the 75160 and 75161 ICs drive GPIB I/O lines. An Atmel (www.atmel.com) AVR AT90S8515 microcontroller provides firmware-resident sequence control and in-circuit-programmable flash memory that simplifies firmware design and upgrades. The USB also can supply 5V of power at as much as 500 mA, which eliminates the requirement for an external power supply. The controller also supports the required low-power mode to reduce consumption to less than 1 mA.

The designers used the Protel (www.altium.com) schematic-capture and pc-board-layout software to design the circuit. They used a milling machine to produce the prototype pc board and partially assembled the board with a manual SMD placer. You can also use a commercial prototype pc-board-fabrication service to prepare a double-sided pc board with plated through holes and manually assemble the circuit. **Figure 2** shows an internal view, and **Figure 3** shows the completely assembled controller, which is easy and fast to build.

The controller communicates with the host computer through a logical serial interface that enables use of the

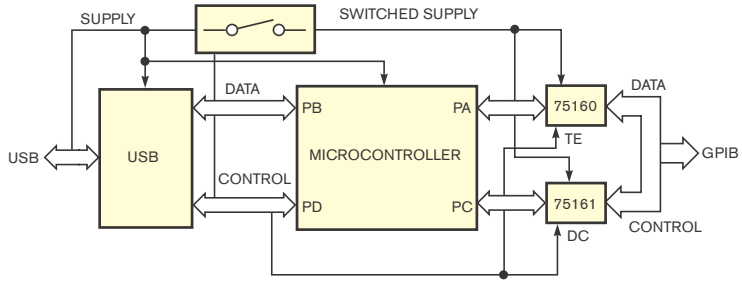

Figure 1 This USB-based GPIB controller requires only four ICs.

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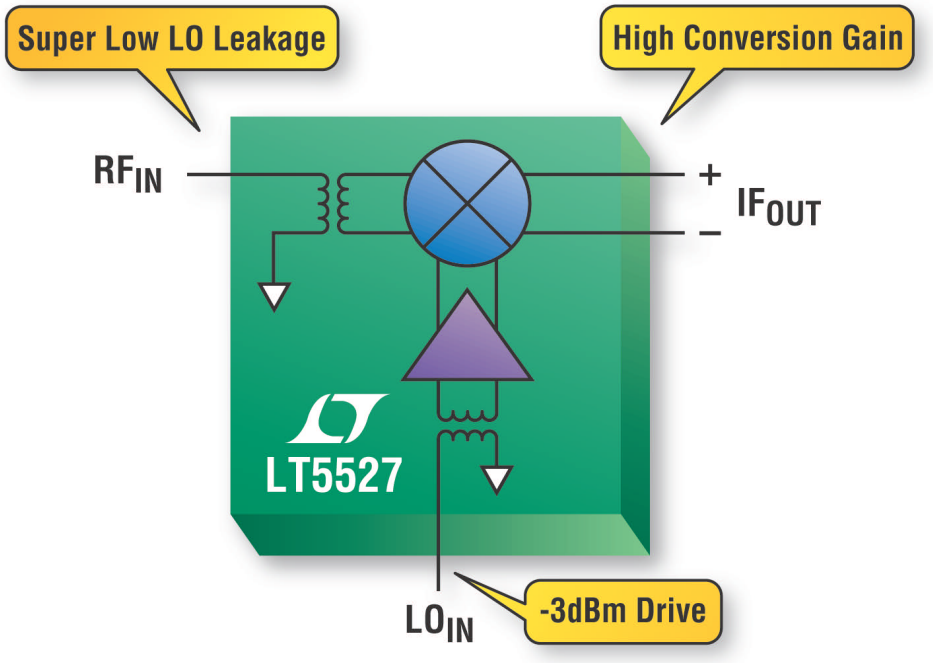

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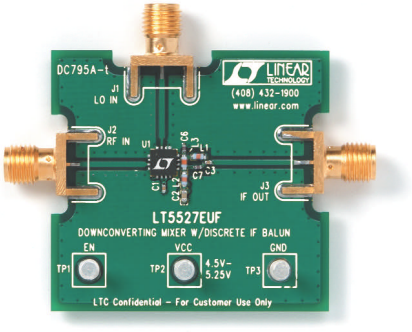
- -44dBm LO-RF Leakage
- Single-Ended, 50Ω RF & LO Inputs

LT5527 Demo Board



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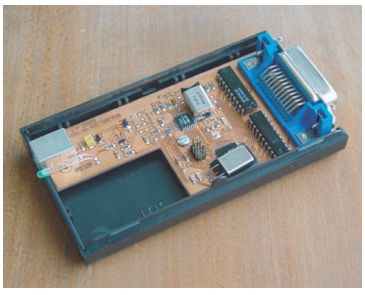

Figure 2 A top view of the controller's pc board shows the USB connector (left) and the GPIB connector (right).

Figure 3 The controller in its housing presents a profile that's not much larger than a GPIB cable connector.

controller with any programming language that supports serial-port communications. The LabView driver is compatible with LabView's built-in GPIB driver, thus simplifying adaptation of programs to the new interface. The driver is a collection of virtual instruments, which require only one more input—that is, a serial-port number—than a built-in GPIB driver.

Thanks to its open-source design, the controller provides a highly cost-effective approach to controlling GPIB instruments that's adaptable to many computational platforms. You can obtain the microcontroller's firmware; descriptions of the protocols; and all other necessary files, including a pc-board layout, at http://lsd.fe.uni-lj.si/gpib/. With that information, you can write a driver for whatever operating system or programming language you choose. In addition, the Web page includes firmware for the Atmel AVR microprocessor, a user's manual for the assembled interface, and additional notes on GPIB and LabView. To download a 1505-kbyte, zip-formatted archive containing the entire project, go to: http://lsd.fe.unilj.si/gpib/complete.zip.EDN

Programs calculate 1% and ratio-resistor pairs

Carl Rutschow, Upland, CA

If you perform analog-circuit design, you'll occasionally need to use a resistor with a nonstandard value to produce a particular gain, ratio, or attenuation factor. You can create resistors of unusual values by connecting two standard-value resistors of 1% tolerance in parallel. Because it is impossible to readily predict which resistor pairs will fall closest to the desired value, a computer program can help by calculating all combinations of standard 1% resistors to determine the best values for your application.

The Visual Basic, compiled, executable file Rratio2.exe checks all standard 1%-resistor values in a given range for a desired ratio, attenuation factor, or noninverting operational-amplifier gain (**Figure 1**). You can download the program from www.edn.com/051216di1. You select the calculation mode via the program's window buttons. As an option, you can choose whether the program displays all possible values or only the values closest to the target value.

Using standard 1%-resistor values, a second program, RPar2a.exe, also available at www.edn.com/051216di1, checks and displays all appropriate combinations that generate a desired parallel resistor's value. The program generally calculates several parallel combination values that fall well within 0.1% of the desired value. By comparison, a single 1% resistor's nominal value may differ by as much as 1.45% from the desired value. Note that, for both programs, the calculated resistance values depend on the paired resistors' tolerances.EDN

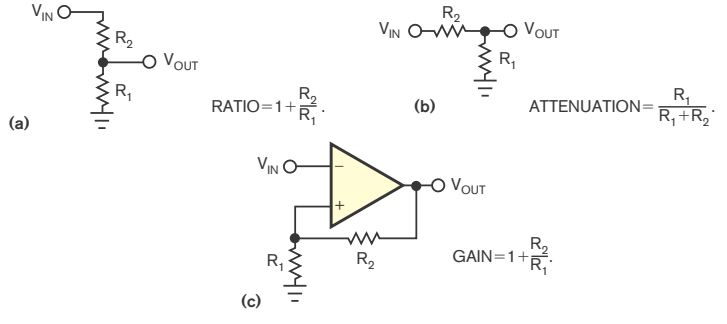

Figure 1 You can use the program Rratio2.exe to calculate ratio (a), attenuation (b), or gain (c).

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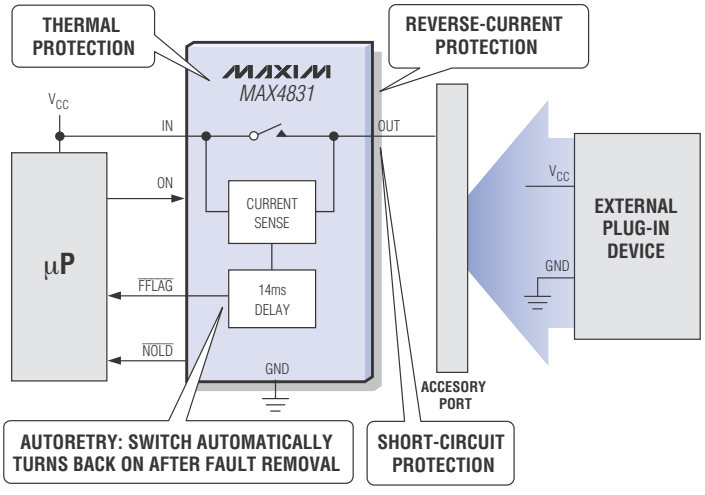

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MAX4828/9	100	0.7	2.3 to 5.5	Yes (5mA limit)	Yes	MAX4829	6-µDFN (1 x 1.5)
MAX4830/1	50	1.4	2.3 to 5.5	Yes (5mA limit)	Yes	MAX4831	6-µDFN (1 x 1.5)
MAX4785/6	50	0.7	2.3 to 5.5	—	Yes	MAX4786	4-/5-SC70
MAX4787/8	100	0.7	2.3 to 5.5	—	Yes	MAX4788	4-/5-SC70
MAX4789/90	200	0.2	2.3 to 5.5	—	Yes	MAX4790	4-SOT143/5-SOT23/6-TDFN
MAX4791/2	250	0.2	2.3 to 5.5	—	Yes	MAX4792	4-SOT143/5-SOT23/6-TDFN
MAX4793/4	300	0.2	2.3 to 5.5	—	Yes	MAX4794	4-SOT143/5-SOT23/6-TDFN
MAX4795/6	450	0.2	2.0 to 4.5	—	Yes	MAX4796	6-SOT23/6-TDFN
MAX4797/8	500	0.18	2.0 to 4.5	—	Yes	MAX4798	6-SOT23/6-TDFN
MAX4772/3	200/500	0.4/0.18	2.0 to 4.5	—	Yes	MAX4773	6-SOT23/6-TDFN

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Simplify worst-case PSpice simulations with customized measurement expressions

Wayne Huang and Jeff Van Auken, Picor Corp, North Smithfield, RI

During IC design, worst-case simulations help designers account for variations in characteristics of PNP and NPN transistors and base and polysilicon resistors. These four classes of devices alone produce more than 16 combinations of simulation conditions. To accommodate temperature variations, each combination undergoes simulation at −40, +27 (room temperature), and +125°C, producing at least 48 series of data to analyze when simulations are complete. To help an IC designer evaluate simulated waveforms' characteristics, PSpice provides a library of ready-to-use, predefined measurements, including bandwidth, gain/phase margins, and more. PSpice also allows a designer to use predefined YatX and XatNthY measurements to measure a waveform's y value at a given x value—usually, time—and to find an x value that corresponds to the nth instance of a given y value (**Reference 1**).

However, when a designer must measure the value of Waveform 1 when Waveform 2 crosses a certain y value, predefined measurements do not apply because, unlike many programming languages, PSpice allows no embedment. This Design Idea describes how to create a customized PSpice measurement expression that solves the problem. As **Listing 1** shows, the measurement expression itself is straightforward. Line 1 finds the X_value (x1) when Trace 1 crosses the y1_value for the nth positive slope. Line 2, denoted by braces { } at the bottom of the **listing**, searches for the value of Trace 2 (y2) at x1. Similarly, **Listing 2** shows how a designer can create a measurement expression to find a y2 value when Trace 1 crosses a y1_value for the nth negative slope or when Trace 1 crosses a given percentage of its full y-axis range.

Figure 1 shows a simulation example in which the input and the output voltages represent a comparator's input and output, respectively. When the input voltage is greater than the positive threshold voltage, then the output voltage is high; when the input voltage is less than the negative threshold voltage, the output voltage is low. Using customized measurement expressions, a designer can easily find the rising and falling thresholds and the comparator's hysteresis voltage for all conditions immediately after the probe data becomes available. If any condition exists in which the threshold doesn't meet the design specification, the designer can then go directly to that condition and spend time on further analysis.

The simulation example describes an input-voltage monitor comprising a comparator that acts as a "power-good" block in a power-management IC. When the input voltage rises above a 13V enable threshold, the output voltage goes high and enables other circuit blocks. When the input voltage falls below a 10V disable threshold, the output voltage goes low and disables other circuits. The difference between the enable and the disable thresholds—that is, 3V—defines the hysteresis voltage. A worst-case simulation of the circuit must account for variations in characteristics of NPN and PNP transistors, base resistors, and polysilicon resistors in the circuit. Each device's characteristics can fall at either the low or the high end of the process specifications and thus produce 16 combinations.

The toolbar lists a few of the 16 possible combinations. For example, LLLL refers to the case in which characteristics of NPN and PNP transistors and base and polysilicon resistors all fall at their low values. In addition, one pass of the simulation uses nominal values; that is, the components' specifications fall in the centers of their nominal characteristics. For each combination, PSpice simulates the circuit's behavior at low, room, and high temperatures, respectively, producing 51 data traces for the block's input and output voltages for a total of 102 displayed traces. After PSpice assembles the data, the circuit's designer must extract the actual threshold voltages for each condition for comparison with the circuit's specifications. Given the large number of displayed traces, using the display's cursor to measure each threshold consumes much of a designer's time. Using a customized PSpice measurement extracts the threshold voltages in a fraction of the time and presents the data in tabular form. The table immediately below the waveform plot contains simulation results for all 51 traces. Columns 1, 2, and 3 list results for nominal characteris-

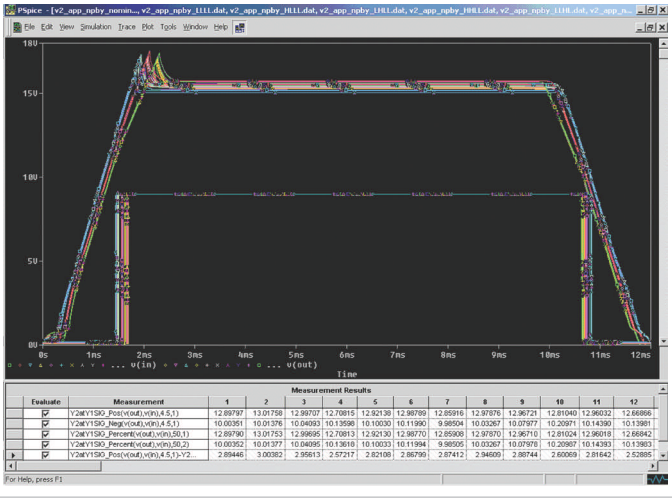

Figure 1 On-screen waveforms represent inputs and outputs for multiple simulation passes.

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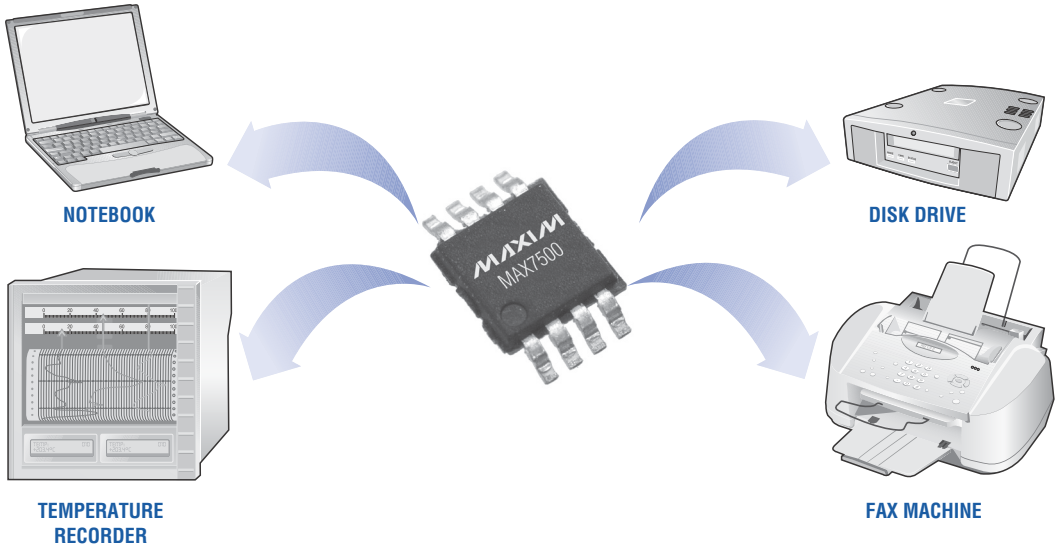

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LISTING 1 MEASUREMENT EXPRESSION FOR x1

View Measurement

```
Y2atY1SIG_Pos(1,2,y1_value,n_occur)= y2
*
*#Desc#* Find the value of trace 2 at the X_value corresponding to the
*#Desc#* nth postive slope crossing the given Y1_value for trace 1
*
*#Arg1#* Name of trace 1
*#Arg2#* Name of trace 2
*#Arg3#* nth occurance
*#Arg4#* Y1 Value
*
  {
    1| search forward for n_occur:level (y1_value, positive) !1;
    2| search forward xval (x1) !2;
  }
```

LISTING 2 MEASUREMENT EXPRESSION FOR y2

```
Y2atY1SIG_Neg(1,2,y1_value,n_occur)=y2
  {
    1| search forward for n_occur:level (y1_value, negative) !1;
    2| search forward Xvalue (x1) !2;
  }

Y2atY1SIG_Percent(1,2,y1_pct,n_occur)= y2
  {
    1| search forward for n_occur:level (y1_pct%  ) !1;
    2| search forward xval (x1) !2;
  }
```

tics, and columns 4, 5, and 6 list results for low, room, and high temperatures when all devices' specifications reside at their lower extremes.

Row 1 of the table displays the measurement expression and results for the enable-voltage threshold. When the output voltage first crosses 4.5V (one-half the simulated circuit's 9V power-supply bus voltage) on the positive slope, the simulation records the value of the input voltage as the enable-threshold voltage, and row 2 measures the disable-threshold voltage. Rows 3 and 4 measure the enable- and disable-threshold voltages by another method: When the output voltage passes 50% of the full-scale value for the first and second times, PSpice measures the value of the input voltage. Row 5 calculates the hysteresis voltage. EDN

REFERENCE

1 *PSpice User's Guide*, Cadence Design Systems Inc, June 2003, www.cadence.com.

Tiny twisted-pair transmission line solves test-fixture woes

Glen Chenier, Allen, TX

Engineers often construct test fixtures that include high-speed differential signals. Although miniature coaxial cable is widely available, there's no commercial off-the-shelf source for small-gauge twisted-pair cable that's suitable for differential signals. Although Category 5 Ethernet cable contains four twisted pairs, it's too large for crowded fixtures and for attachment to the Amp Z-Pack connectors some fixtures require. Many engineers are unaware that they can twist together two lengths of AWG #30 Kynar-insulated wire—garden-variety wire-wrap and prototype cut-and-jumper wire—to make a 102Ω differential-transmission line. If you use Kynar's dielectric constant and the insulation's thickness to compute its properties, the line's calculated differential impedance works out to 110Ω. In practice, differential TDR (time-domain-reflectometer) measurements show that the line's actual impedance consistently measures 102Ω—only 2% away from the target impedance and thus close enough for most practical purposes.

To make your own twisted pair, start with a long AWG #30 Kynar-insulated wire and fold it in half. Enlist a coworker to hold the cable's closed end by slipping the loop around a screwdriver's blade. If you're working alone, slip the loop around a doorknob. Tightly twist the two wires' free ends together and insert the twisted ends into the chuck of a Dremel (www.dremel.com) rotary tool. Tighten the chuck and hold the Dremel tool so that the wires are stretched tightly, are of the same length, and lie parallel with each other.

Apply a slight amount of tension to the wires and start the tool. As the wires twist together, the pair shortens and pulls the tool's operator toward the loop support. A variable-speed Dremel tool works best when you operate it at its slowest setting. If you have only a fixed-speed Dremel tool, avoid overtwisting the wires by preparing a length of 10 to 20 ft of cable at a time. The extra length allows time to switch the tool off and avoid overtwisting the wires. Cut off and discard the cable's nonuniformly twisted end sections.

The amount of twist in the wires is not critical, but the wires should be firmly twisted together. Using approximately eight to 10 twists/in. works well. To count the twists, hold a portion of the cable against a ruler or measuring scale under a magnifier and count 16 to 20 "bumps," or half-twists, per inch. Using too many twists per inch uses excess wire and increases losses and propagation delay. For the lengths in a test fixture, losses are insignificant except at extremely high frequencies.

You can also use a variable-speed hand drill with a 1/4- or 3/8-in. chuck to twist the wires, but you need to fold the wires' free ends several times and wrap them in duct tape to ensure a snug fit in the drill's chuck. When using any power tool, wear safety glasses or other eye protection during the procedure. EDN

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productroundup

CIRCUIT PROTECTION

3.3V ESD protection device targets systems transitioning from 5V

Providing pin compatibility with 5V protection devices, the µClamp-3304A 3.3V ESD (electrostatic-discharge)-protection device allows simplified board design in industrial-equipment, computer, and portable-communication designs. Providing protection for four lines from ESD, the device features a low-leakage current and a low clamping-voltage range. The SC-89 package measures 1.7×1.7×0.6 mm and fits into SOT-666- or SC-89-based 5V designs, providing reliability at a less-than-5V level. The ESD-protection device costs 28 cents (1000).

Semtech Corp, www.semtech.com

Slow-blow surface-mount fuses guard against frequent power surges

Targeting use in systems with frequent surges, these slow-blow, surface-mount fuses come in a 1206 form-factor chip size. Clear time characteristics of the fuses include 100% rated current at a four-hour minimum; 200% rated current at a 1-sec minimum, 120-sec maximum; 300% rated current at a 0.1-sec minimum, 3-sec maximum; and 400% rated current at a 0.002-sec minimum, 0.05-sec maximum. The ROHS (reduction-of-hazardous-substances)-compliant surface-mount fuses cost 30 cents (100,000).

Raychem Circuit Protection, www.circuitprotection.com

CIRCUIT PROTECTION

SMD fuse features breaking capacity of 100A at 250 and 277V

The UMT250 SMD fuse features breaking capacities of 200A at 250 and 277V ac or 100A at 125V dc over a current range of 315 mA to 4A. measuring 10×3×3 mm, the fuse takes up 80% less volume than a typical microfuse or a 5×20-mm-cartridge fuse. The ROHS (reduction-of-hazardous-substances)-compliant SMD fuse costs 56 cents (100).

Schurter, www.schurter.com

Thin-film fuse features stable characteristics

The miniature 0402-sized TF10A thin-film fuse quickly responds to unwanted circuit inputs. It provides overcurrent protection for circuit clocks in electronic devices and features an internal resistance of 320 to 35 mΩ, low power consumption, and low voltage drop. The product has a rated voltage of 24V and a rated current of 0.05 to 2.50A. The TF10A costs $360 (1000).

KOA Speer Electronics Inc, www.koaspeer.com

Protection thyristor provides a range of current ratings

The Teccor Q2L series SIDACtor thyristor measures 1 mm high and features 54% less pc-board space and a 51% smaller profile than the vendor's DO-214AA. The protection thyristor provides bidirectional transient-voltage protection and peak-to-peak current ratings of 75A for a 5×310/10×700-µsec event with an ITU/YDT waveform, 80A for a 10×1000-µsec event with a GR 1089 waveform, and 100A for a 10×560-µsec event with a TIA-968 waveform. The series complies with ROHS (reduction-of-hazardous-substances) regulations.

Littelfuse Inc, www.littelfuse.com

Quick-acting-fuse series has a 50A breaking capacity

Quick-acting fuses in the thin-film, flat-chip MFU series feature 5A rated-current values and stability in accordance with UL 248 14 and IEC 60127 4. The MFU 0603 and MFU 0805 have a 0.5 to 4A current range with a 32V rated voltage; the MFU 0805 has a 5A rated current and a 63V rated voltage. At these voltages, the devices feature a 50A breaking capacity. MFU fuses cost 17 to 37 cents (5000), based on size and value of the rated current.

Vishay Intertechnology Inc, www.vishay.com

MICROPROCESSORS

IEM software combines energy management, frequency scaling

The Nucleus EM (energy manager) combines ARM IEM (intelligent-energy-management) software technology and DVFS (dynamic-voltage-and-frequency-scaling) hardware. The product enables the use of the IEM technology at the RTOS level. Available in source-code format without royalty fees, Nucleus software licenses cost $12,495 per seat.

Accelerated Technology, www.acceleratedtechnology.com

32-bit microcontroller series supports CAN and LIN

The vendor based its MB91270 microcontrollers on a 32-bit FR-60lite CPU core with internal clock speeds of 32 MHz. The units incorporate a 24-channel ADC and support CAN (controller-area networking), seven channels of LIN (local-interconnect network) configurable as SPI (serial peripheral interface) or UART, and three channels of I^2C. The series includes the MB91F272, featuring a main clock and a subclock, and the MB92F1272S, with only a main clock.

The devices are compatible with the vendor's 16-bit MB90340A microcontroller series, allowing the use of the same basic pc-board design for developing control units requiring more CPU performance. The MB91270 series are available in QFP-100 packages and cost $8.85.

Fujitsu Microelectronics America Inc, http://us.fujtsu.com

Graphics-programming tool adds on to audio-system processors

The DSP Conductor graphical-programming tool suits the vendor's CS4961XX CobraNet-based audio-system processors. The tool lets users drag and drop audio-processing blocks, and it calculates and reports the DSP resource usage before delivering the code. The vendor plans to extend the DSP Conductor's programming features to 32-bit audio DSP families for consumer markets. DSP Conductors are complimentary with the purchase of the vendor's CS-4961XX audio-system-processor ICs.

Cirrus Logic, www.cirrus.com

Security processor suits SME-networking equipment

The single-chip, ARMv4-compliant SafeXcel-5140 RISC processor integrates embedded security acceleration and provides full-duplex, 45-Mbps performance for small packets and full-duplex, 100-Mbps performance for average-sized or large packets. Features include hardware implementations for 3DES, AES, SHA-1, and MD5; a random-number generator; and public-key acceleration. The enterprise security processor also includes packet filtering and flow processing; NAT, NAT-T, NAPT, IPSec, and SRTP (secure-real-time-transport-protocol) processing; and SHA-256, AES GCM (Galois Counter Mode), ASE-XCBC-MAC-96, and extended-sequence numbers. Dedicated IPSec packet-processing hardware reduces power consumption. The SafeXcel-5140 costs $40.

SafeNet, www.safenet-inc.com

Software has DSL capabilities for integrated designs

Rhapsody 6.1 DSL software targets systems with drawing and design equipment requiring compliance with SysML (systems-modeling-language) version 0.91. The Systems Designer version also features simulation capability through a GNU compiler installation, an action-language-mapping guide, and a simulation-menu item. The product generates C code that complies with MISRA (Motor Industry Software Reliable Association) standards.

I-Logix, www.ilogix.com

productroundup

MICROPROCESSORS

Audio engine adds aacPlus support

The Xtensa HiFi 2 audio engine uses Coding Technologies' (www.codingtechnologies.com) aacPlus Version 2 codec engine, a superset of Version 1. The engine supports SBR and AAC-LC. Designers must license the Xtensa HiFi 2 audio engine and the accompanying Xtensa LX processor. The AAC-LC decoder costs $44,000.

Tensilica Inc, www.tensilica.com

8-bit microcontroller family can use 3 or 5V power supplies

Using a 3 or 5V power supply, the 8-bit F_2MC-8FX family includes the 28-pin MB95F136H unit. It offers 32 kbytes of flash memory and 1 kbyte of RAM; an eight-channel, 10-bit ADC; eight external interrupt inputs; 19 I/O ports; and support for two channels of UART, LIN (local-interconnect-network), or serial-I/O interfaces. Features of the 100-pin MB95F128H include 60 kbytes of dual-operation flash with two memory banks; 2 kbytes of RAM; a 12-channel, 10-bit ADC; and support for LIN, UART, and I^2C interfaces. The 48-pin MB95F118H provides 60 kbytes of flash and 2 kbytes of RAM; an eight-channel, 10-bit ADC; and eight external interrupts. The microcontrollers come with a development kit comprising the MB-2146-301, an evaluation board for development with 3V power supplies, the MB-2146-303, and a board for a 5V combination with the MB2146-09 functioning as the interface adapter from the PC USB port. The MB95F136H, MB95128H, and MB95F118H cost $4.50, $7.25, and $5.45, respectively, and come in small-outline packages, low-power QFPs, and QFPs.

Fujitsu Microelectronics America Inc, www.fujitsu.com/us

TEST & MEASUREMENT

Long-distance TAP connection features Gigabit Ethernet

Using communication links, the TapCommunicator suits remote, high-fidelity communications of boundary-scan-test vectors and device-programming data. Systems running boundary-scan applications in the production or service industries must be close to the target or unit under test, often requiring the boundary-scan controller and target pc boards or subsystems to collocate and also to support widespread corporate-test topologies. The product includes an uplink and a downlink module for coding and decoding the boundary-scan applications and is compatible with the IEEE-standard 802.3z, 1998 (Gigabit Ethernet), and IEEE 1149.1. Operating on IEEE 1149.1 protocols and state machines allows the device to be vendor-independent and allows its use with any compliant tester, emulator, or programmer product.

JTAG Technologies, www.jtag.com

Dedicated test devices target MIMO WLAN technologies

The wireless IQnxn MIMO (multiple-in/multiple-out) test system and the One-Box tester MIMO add-on-software package for IQview and IQflex instruments find use in advanced MIMO wireless-LAN products. Targeting IC and product developers, the IQnxn provides flexibility for expandable arrays of integrated and synchronized VSAs (vector-signal analyzers) and VSGs (vector-signal generators) for wireless products. Running on the IQview or the IQflex test platform, the One-Box tester executes production-

test programs using advanced analysis techniques, delivering test times close to non-MIMO products. An IQnxn MIMO test system in a starter configuration costs $147,500, an IQnxn MIMO expansion unit costs $59,000, and a One-Box tester MIMO add-on-software-package single-user license costs $5995.

LitePoint Corp, www.litepoint.com

Handheld spectrum analyzer takes radiation measurements

The 9102 handheld spectrum analyzer, targeting network operators, broadcast stations, regulation authorities, and engineering offices, tests actual radiation against defined limits. The 9131 EMF (electromagnetic-field)-measurement option allows EMC (electromagnetic-compatibility) measurements and supports spectrum- and network-analysis applications. Antennas for various applications are optional. The 9102 with the 9131 EMF-measurement option costs $9000.

Willtek Communications, www.willtek.com

EDA TOOLS

CE-ATA simulation models target "Mikey"

Suiting Hitachi's 8-Gbyte Microdrive, "Mikey," CE-ATA simulation models allow designers to simulate interaction between CE-ATA product designs and microdrive-based devices at the presilicion stage of chip development. Simulation models are available to select customers.

Denali Software, www.denali.com

Layout- and logic-design translators port design environments

Two translators port designs for Protel's design environment to the vendor's tools. A logic translator allows designers to import individual Protel design files into the vendor's Pantheon pc-board-layout tool, and the logic translator can import Protel logical files into the vendor's Mozaix schematic-capture, design-entry tool. Both devices use Protel ASCII files in the import process. Layout and logical translators for Protel-based designs are available on HPUX, Sun Solaris, Linux, and Windows platforms and cost $5000.

Intercept Technologies Inc, www.intercept.com

Upgraded pc-board suite provides LabView software compatibility

Series 9 of the vendor's EWB (Electronics Workbench PC-

productroundup

EDA TOOLS

Board group) DesignSuite provides pc-board tools compatible with the vendor's LabView testing software. The suite allows the EWB MultiSim simulation environment to exchange files with LabView and acquire real-world data in LabView and apply it to MultiSim simulations. Designers can import simulation results into LabView or SignalExpress in their native formats and use the results as benchmarks during testing and debugging. Additional features include the ability to use mathematical expressions within analyses during simulation, circuit wizards that automatically generate circuitry to match user-defined parameters for op amps and MOSFET amplifiers, and the ability to prioritize routing order by net or routing a single net in the Ultiroute 9 autorouter.

National Instruments, www.ni.com

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realitycheck

YESTERDAY'S HYPE MEETS TODAY'S REALITY

STATS Expected sales: 6 million units / Actual sales: approximately 2 million units

Phone/game combo fails to engage an audience

Launched amid fanfare in 2003, Nokia's N-Gage melded a mobile phone with a handheld game machine. Last month, the company quietly admitted it had sold only a third of the 6 million units it expected to ship over three years and announced it would cease development. What went wrong? Although the logic of combining two popular devices seemed sound, the company managed to produce a whole that users perceived as considerably less than the sum of its parts.

In addition to a dearth of compelling games and a high price, two design quirks doomed the machine. First, the user had to open the battery compartment to insert a new game card—an astonishing inconvenience. Second, in an apparent attempt to keep the display free of smears from the user's cheek, Nokia positioned the phone microphone and speaker along one edge of the housing, thus forcing the user to hold the device perpendicular to the face when talking. Incredulous consumers immortalized their disdain in a sarcastic Web site (check out the photo galleries at www.sidetalkin.com), and not even a subsequent redesign that alleviated the "taco-talking" position could help N-Gage recover any cachet.—by Matthew Miller

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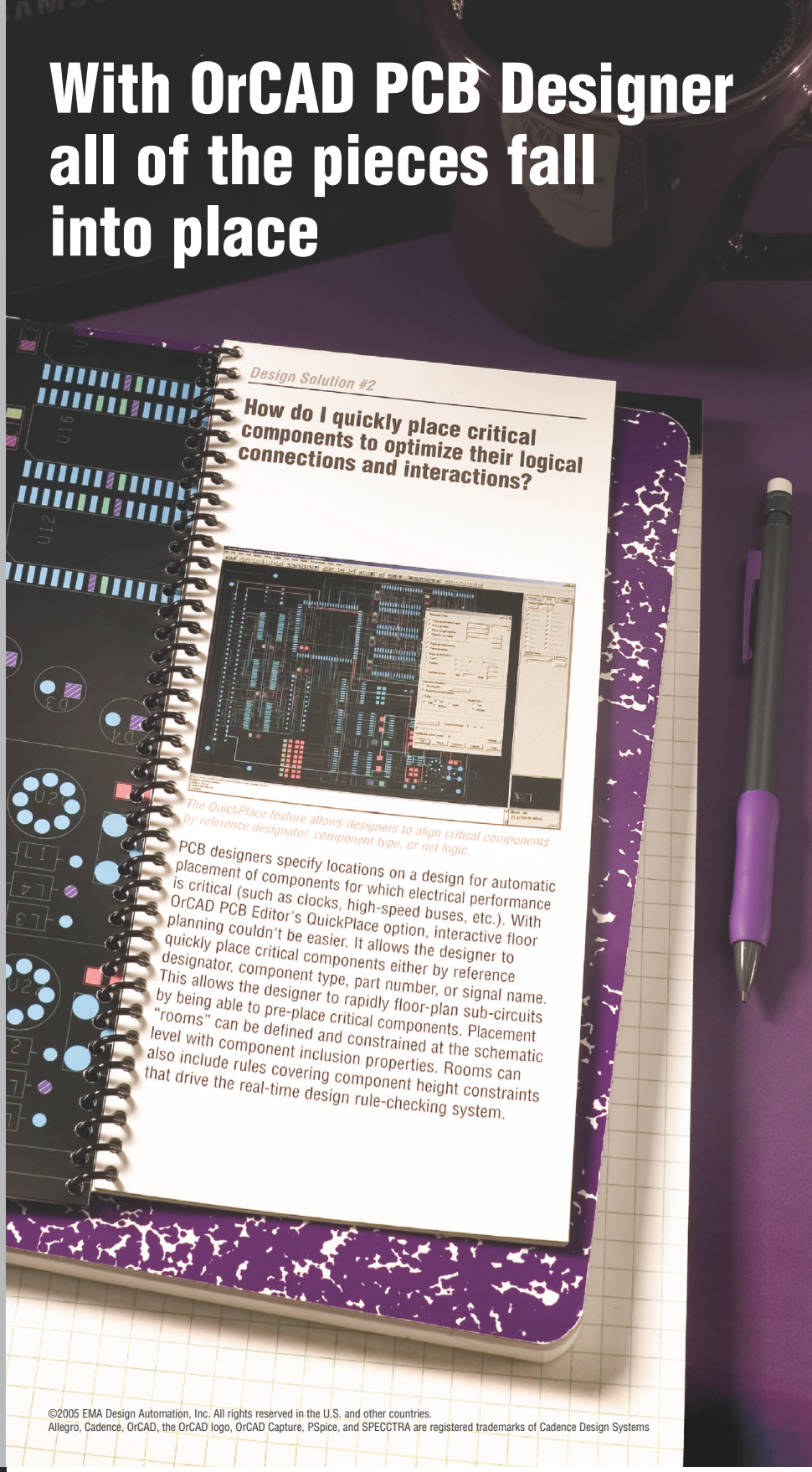

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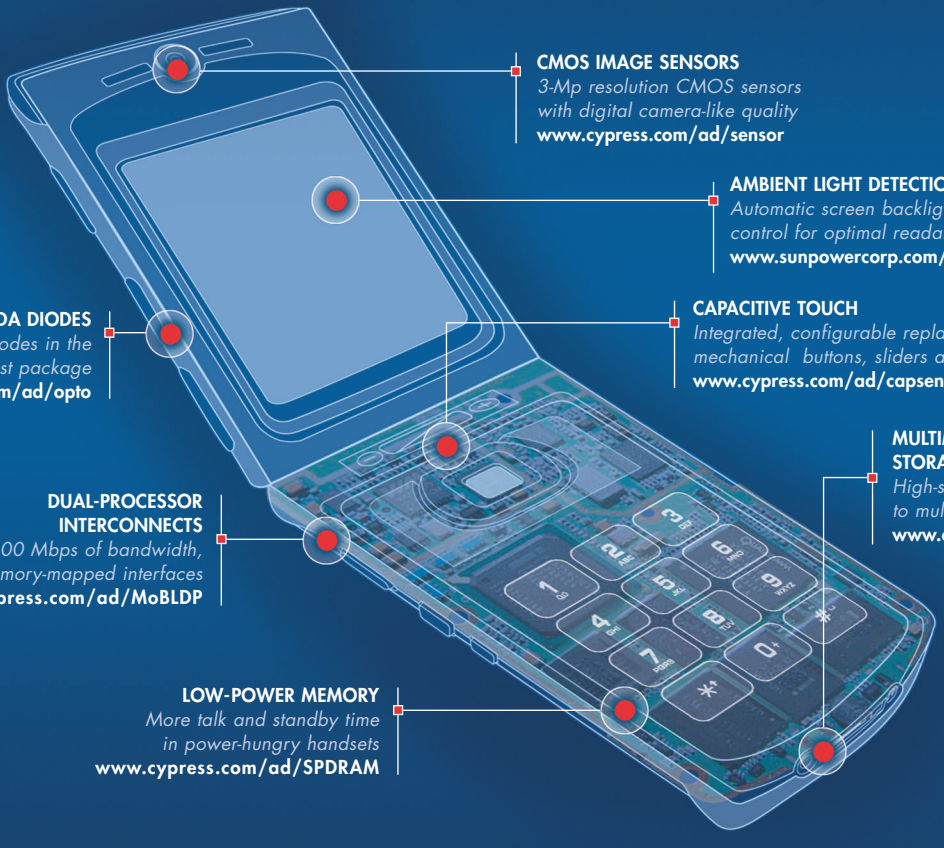

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